

COMPAL CONFIDENTIAL

MODEL NAME : **CAP10**

PCB NO : **LA-E321P**

BOM P/N : **451A4X31L01**

GPIO MAP: **Gen7 GPIO Master_XXXX**

CRANE17

Kaby Lake H-type (2 chip)

REV : 1.0(A00)

2016.11.30

@ : Nopop Component

EMC@ : EMI/ESD/RF part

CONN@ : Connector Component

XDP@ : Total debug Component (pop them until ST)

TB@ : Thunderbolt function

Layout Dell logo



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REV: X00
PWB: XXXXX
DATE: 1403-06

PCB 1TT LA-E321P REV1 MB

Part Number	Description
DAA000CT010	PCB 1TT LA-E321P REV1 MB

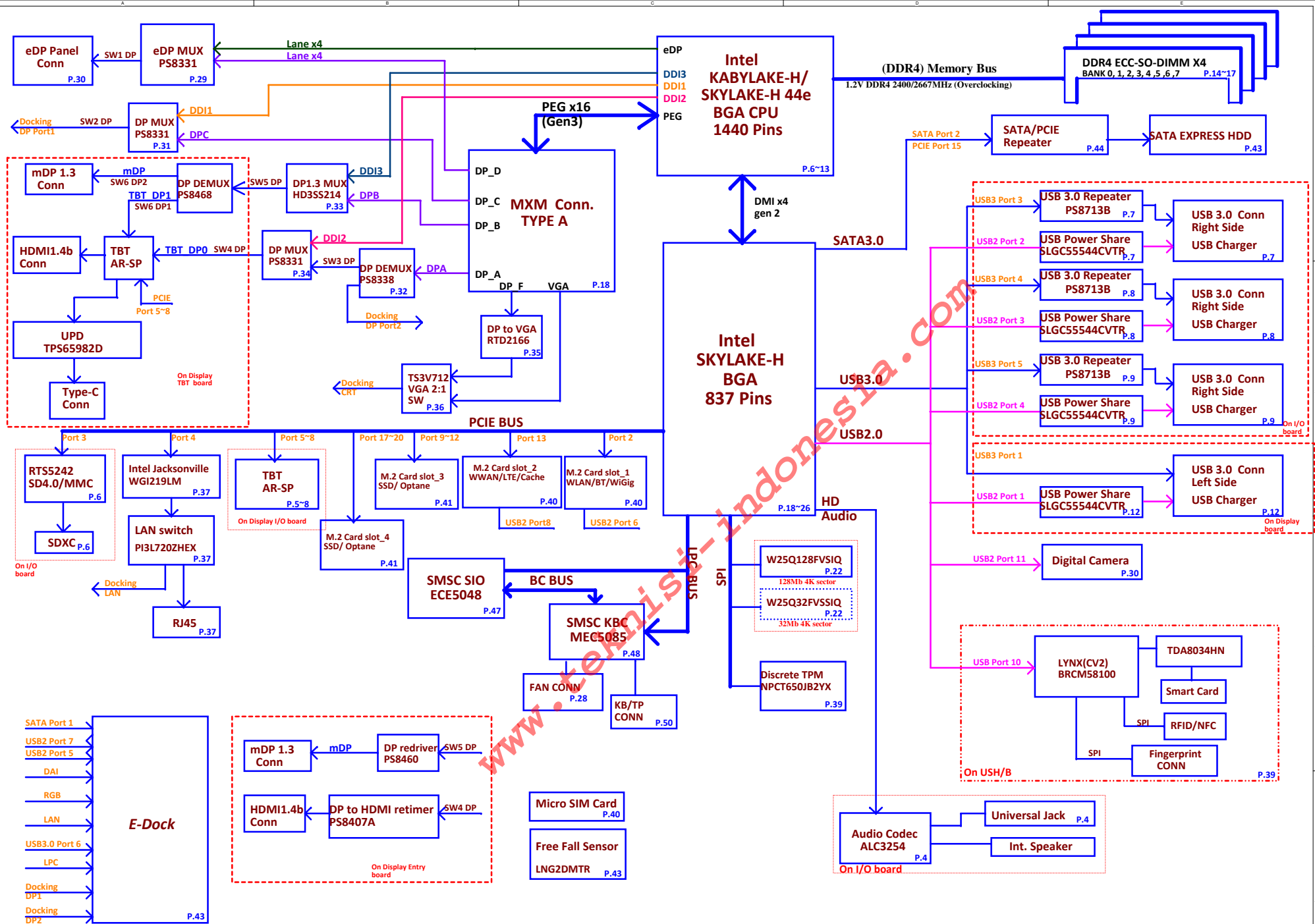
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Cover Sheet			
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Block Diagram

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POWER STATES

Signal State	SLP S3#	SLP S4#	SLP S5#	S4 STATE#	SLP M#	ALWAYS PLANE			RUN PLANE	CLOCKS
S0 (Full ON) / M0	HIGH	HIGH	HIGH	HIGH	HIGH	ON	ON	ON	ON	ON
S3 (Suspend to RAM) / M1	LOW	HIGH	HIGH	HIGH	HIGH	ON	ON	ON	OFF	OFF
S4 (Suspend to DISK) / M1	LOW	LOW	HIGH	LOW	HIGH	ON	ON	OFF	OFF	OFF
S5 (SOFT OFF) / M1	LOW	LOW	LOW	LOW	HIGH	ON	ON	OFF	OFF	OFF
S3 (Suspend to RAM) / M-OFF	LOW	HIGH	HIGH	HIGH	LOW	ON	OFF	ON	OFF	OFF
S4 (Suspend to DISK) / M-OFF	LOW	LOW	HIGH	LOW	LOW	ON	OFF	OFF	OFF	OFF
S5 (SOFT OFF) / M-OFF	LOW	LOW	LOW	LOW	LOW	ON	OFF	OFF	OFF	OFF

PM TABLE

State	power plane	+PWR_SRC +5V_ALW +3.3V_ALW +3.3V_ALW2 +3.3V_ALW_DSW +3.3V_ALW_PCH +3.3V_RTC_LDO +1.8V_ALW +1.0V_PRIM	+3.3V_SUS +1.2V_MEM +2.5V_MEM +1.0V_VCCST	+5V_RUN +3.3V_RUN +1.5V_RUN +0.675V_DDR_VTT +3.3V_MXM +5V_MXM +MXM_PWR_SRC	(M-OFF) +VCC_CORE +VCC_EDRAM +VCC_EOPIO +VCC_GTU +VCC_GT +1.0V_VCCSTG +VCC_SA
S0		ON	ON	ON	ON
S3		ON	ON	OFF	OFF
S5 S4/AC		ON	OFF	OFF	OFF
S5 S4/AC don't exist		OFF	OFF	OFF	OFF

SATA	DESTINATION
SATA 0	2280 SSD
SATA 1	Dock
SATA 2	
SATA 3	SATAe HDD
SATA 4	2280 SSD
SATA 5	

Stack up

Layer No.	Name	Er	Material	Thickness (Material SPEC.) Unit : mil
			SolderMask	IT-158
			Add Plating	
1	Top	3.7	Copper foil	0.5oz
2	GND/PWR	3.7	Prepreg	1080
			Copper foil	1oz
3	Sig 1	4.1	Core	4mil
			Copper foil	1oz
4	GND/PWR	3.7	Prepreg	2116Mx2
			Copper foil	1oz
5	Sig 2	3.8	Core	4mil
			Copper foil	1oz
6	Sig 3	3.7	Prepreg	1080Hx2
			Copper foil	1oz
7	GND/PWR	4.1	Core	4mil
			Prepreg	2116Mx2
8	Sig 4	3.7	Copper foil	1oz
			Core	4mil
9	GND/PWR	3.7	Copper foil	1oz
			Prepreg	1080
10	Bottom		Copper foil	0.5oz
			Add Plating	
			SolderMask	
Overall Thickness (1.45mm ± 10%)				57.09

USB3.0	DESTINATION
Port 1	Left Side JUSB1
Port 2	M.2 Slot-2 (WWAN/LTE/Cache)
Port 3	Right Side JUSB1
Port 4	Right Side JUSB2
Port 5	Right Side JUSB3
Port 6	Docking

PCH	USB PORT#	DESTINATION
	1	Left Side JUSB1
	2	Right Side JUSB1
	3	Right Side JUSB2
	4	Right Side JUSB3
	5	Docking USB3.0
	6	M.2 Slot-1 (BT)
	7	Docking USB 2.0
	8	M.2 Slot-2 (WWAN/LTE/HCA)
	9	NA
	10	USH
	11	Camera
	12	NA
	13	NA
	14	NA

USH		
	0	BIO
	1	NA

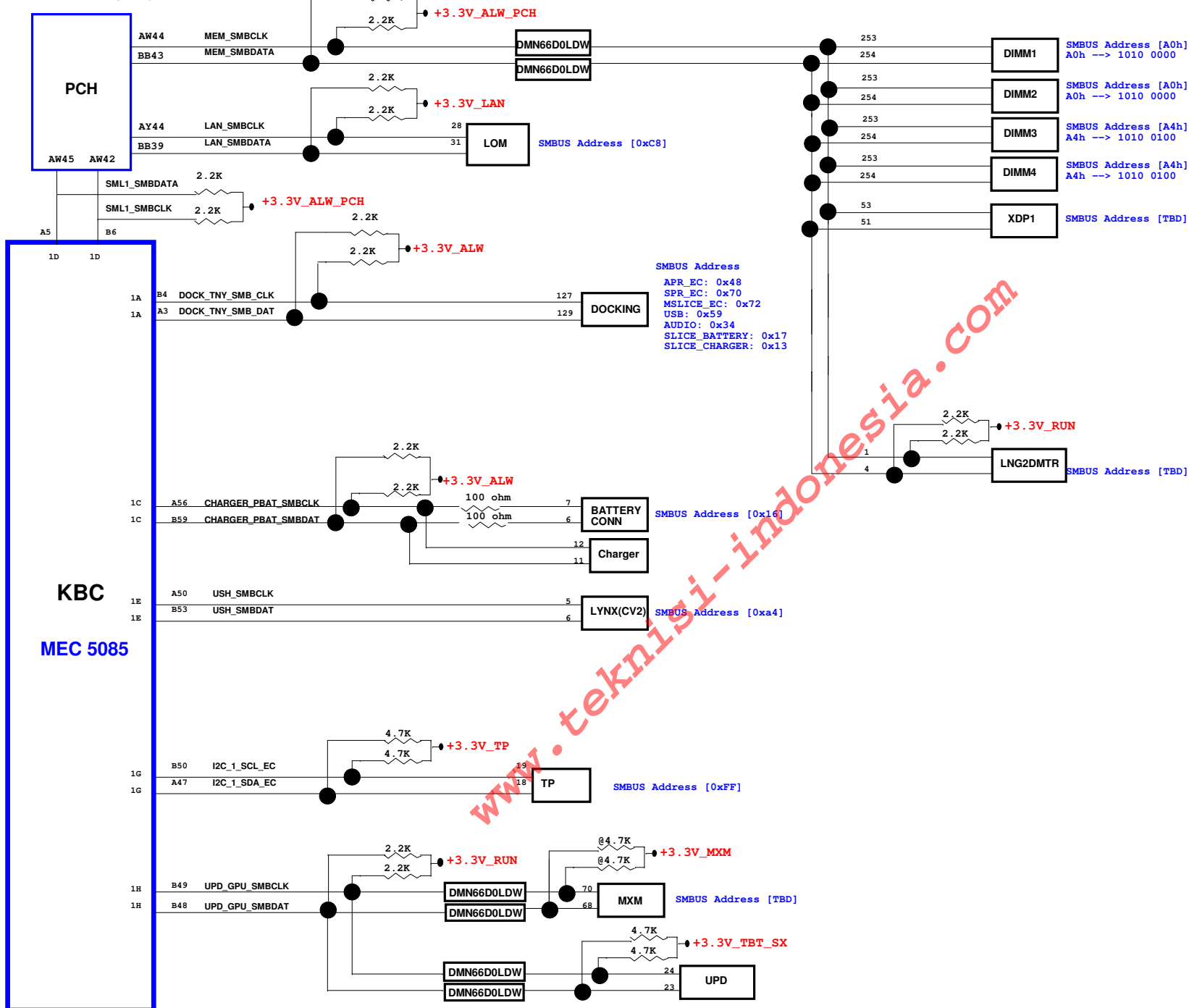
PCI EXPRESS	DESTINATION
Lane 1	NA
Lane 2	M.2 Slot-1 (WLAN/Wigig)
Lane 3	MMI(Card reader)
Lane 4	10/100/1G LOM
Lane 5~8	TBT-Alpine Ridge
Lane 9~12	SSD 2280/ Optane
Lane 13	M.2 Slot-2 (WWAN/LTE/Cache)
Lane 15~16	HDD SATA-Express
Lane 17~20	SSD 2280/ Optane

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SMBUS Address [0x9a]



SMBUS Address
SMB_ADM1032: 0x98
SMB_DIAG_DUMP: 0x04
SMB_DIAG_DUMP2: 0x05
SMB_BLACKTOP: 0x60

SMBUS Address
APR_EC: 0x48
SPR_EC: 0x70
MSlice_EC: 0x72
USB: 0x59
AUDIO: 0x34
SLICE_BATTERY: 0x17
SLICE_CHARGER: 0x13

SMBUS Address [0x16]

SMBUS Address [0xa4]

SMBUS Address [0xFF]

SMBUS Address [TBD]

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SMBUS Boick Diagram

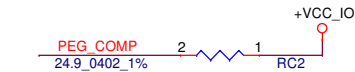
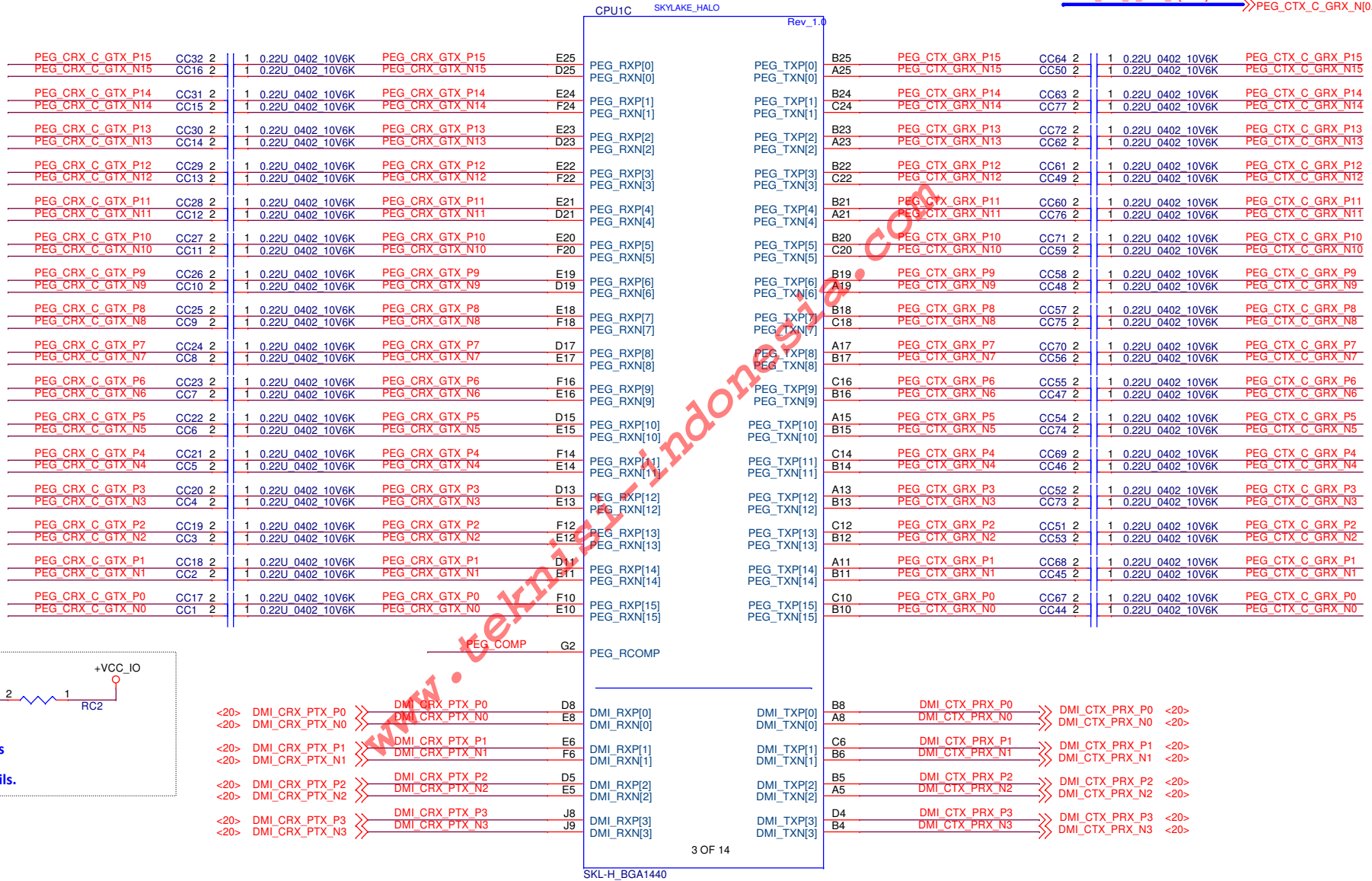
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Size Document Number LA-E321P

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PEG_CRX_C_GTX_N[0..15] << PEG_CRX_C_GTX_N[0..15] <18>
PEG_CTX_C_GRX_P[0..15] >> PEG_CTX_C_GRX_P[0..15] <18>
PEG_CTX_C_GRX_N[0..15] >> PEG_CTX_C_GRX_N[0..15] <18>



CAD Note:
Trace width=12 mils
Spacing=15mil
Max length= 400 mils.

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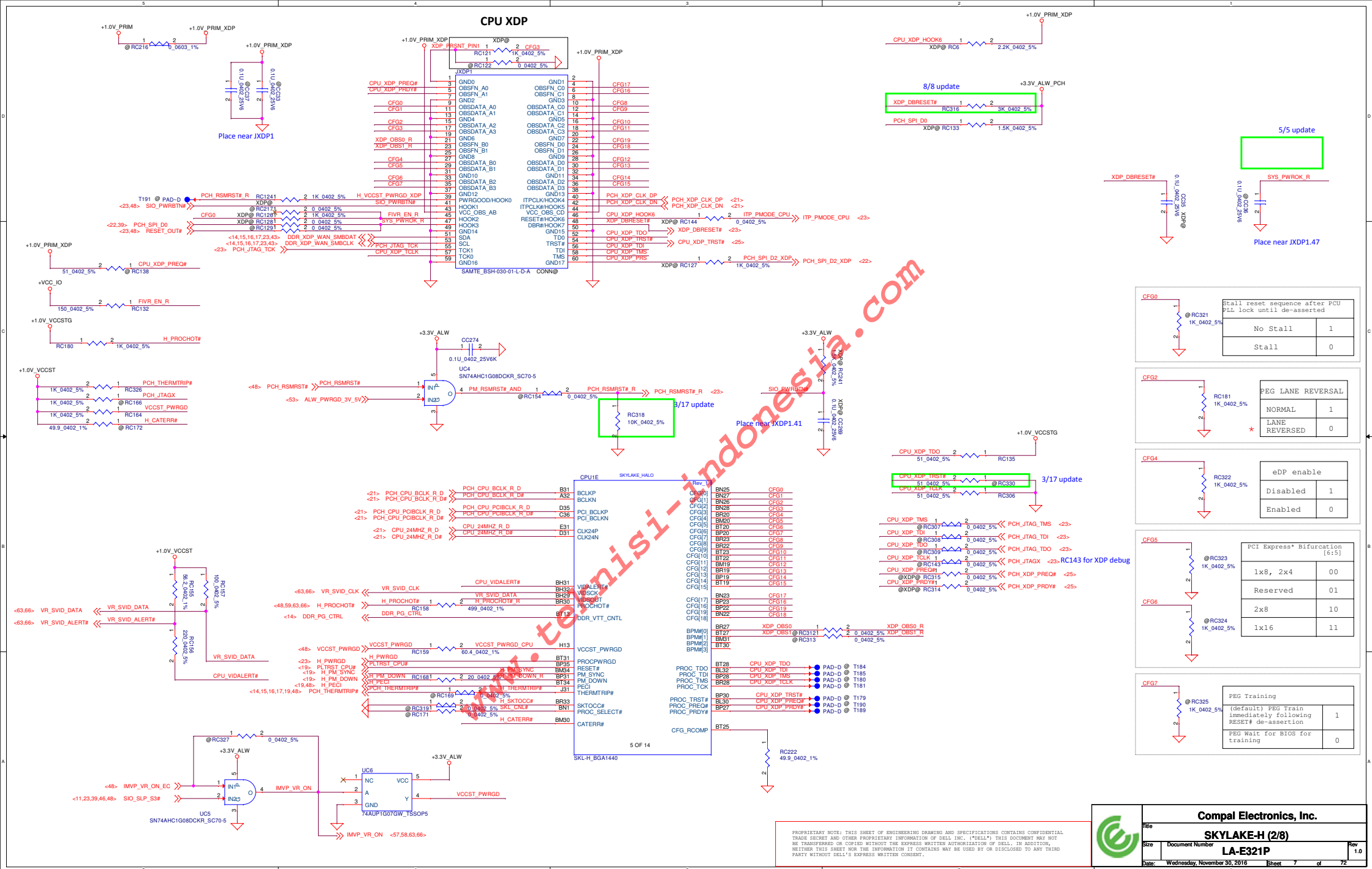


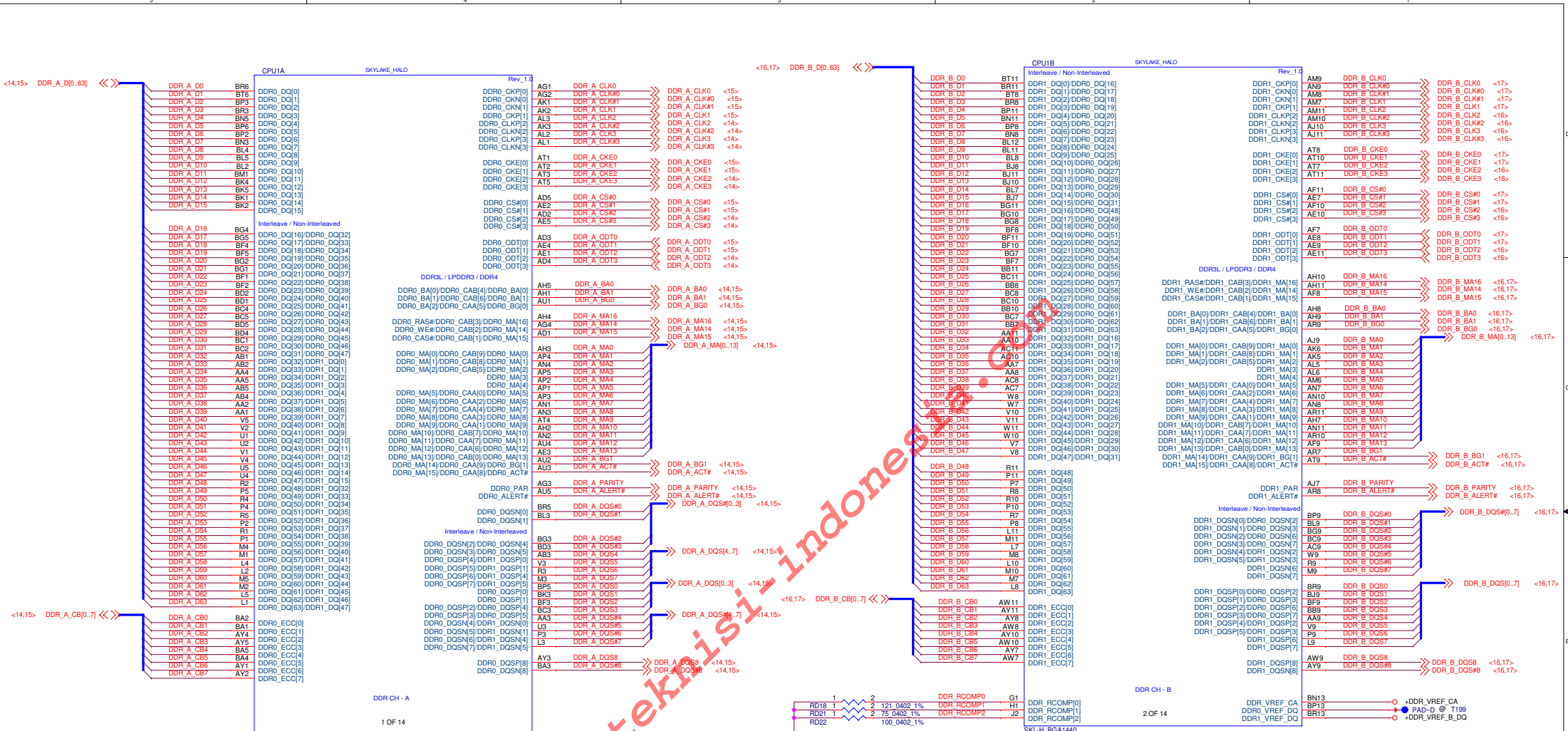
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SKYLAKE-H (1/8)

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Dock Port1

TBT

mDP/TBT

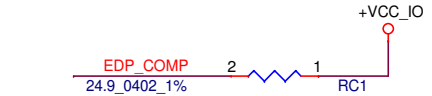
CPU1D SKYLAKE_HALO

Rev_1.0

SKL-H_BGA1440

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COMPENSATION PU FOR
eDP



CAD Note: Trace width=20 mils
Spacing=25mil,
Max length=100 mils.

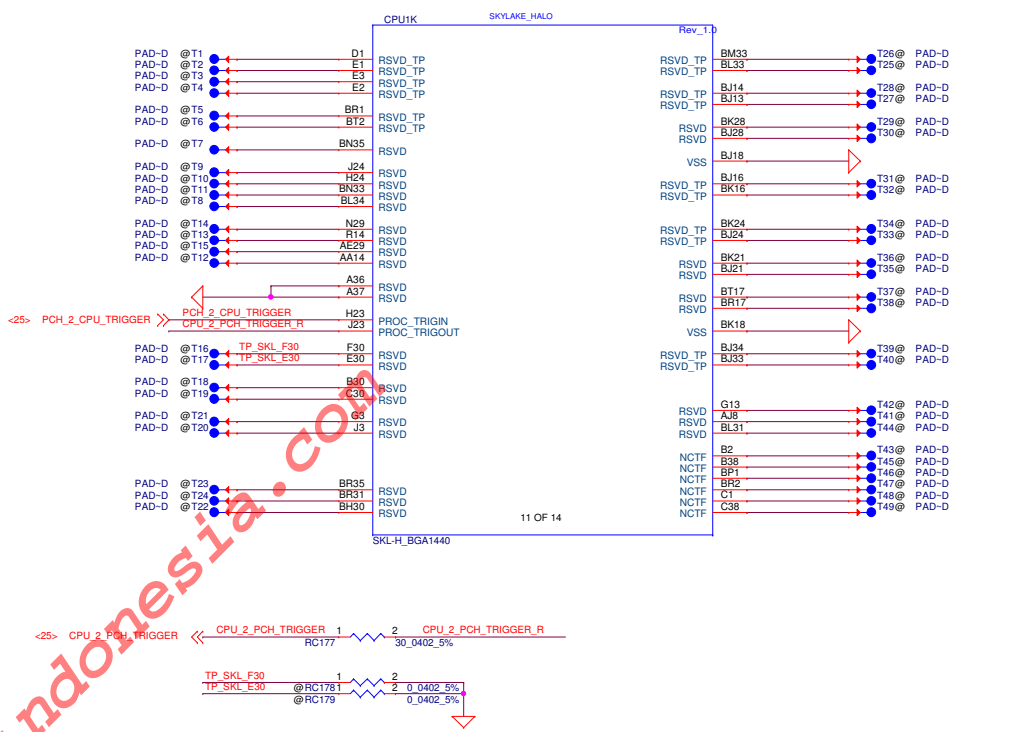
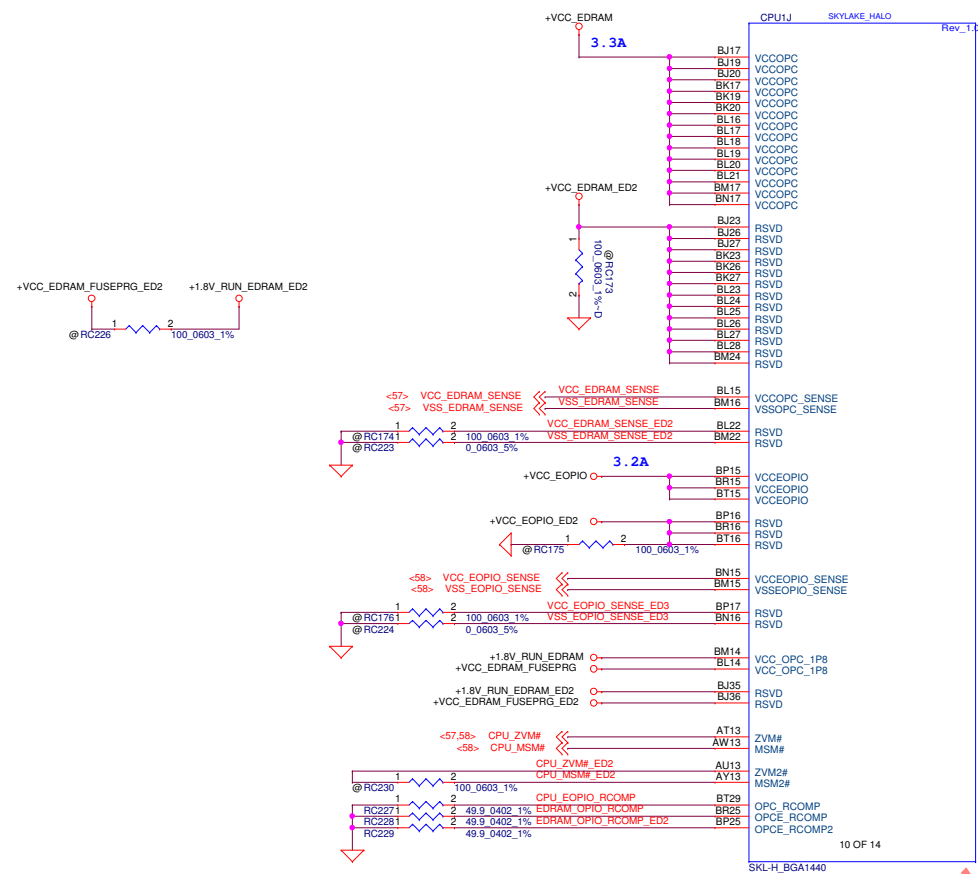


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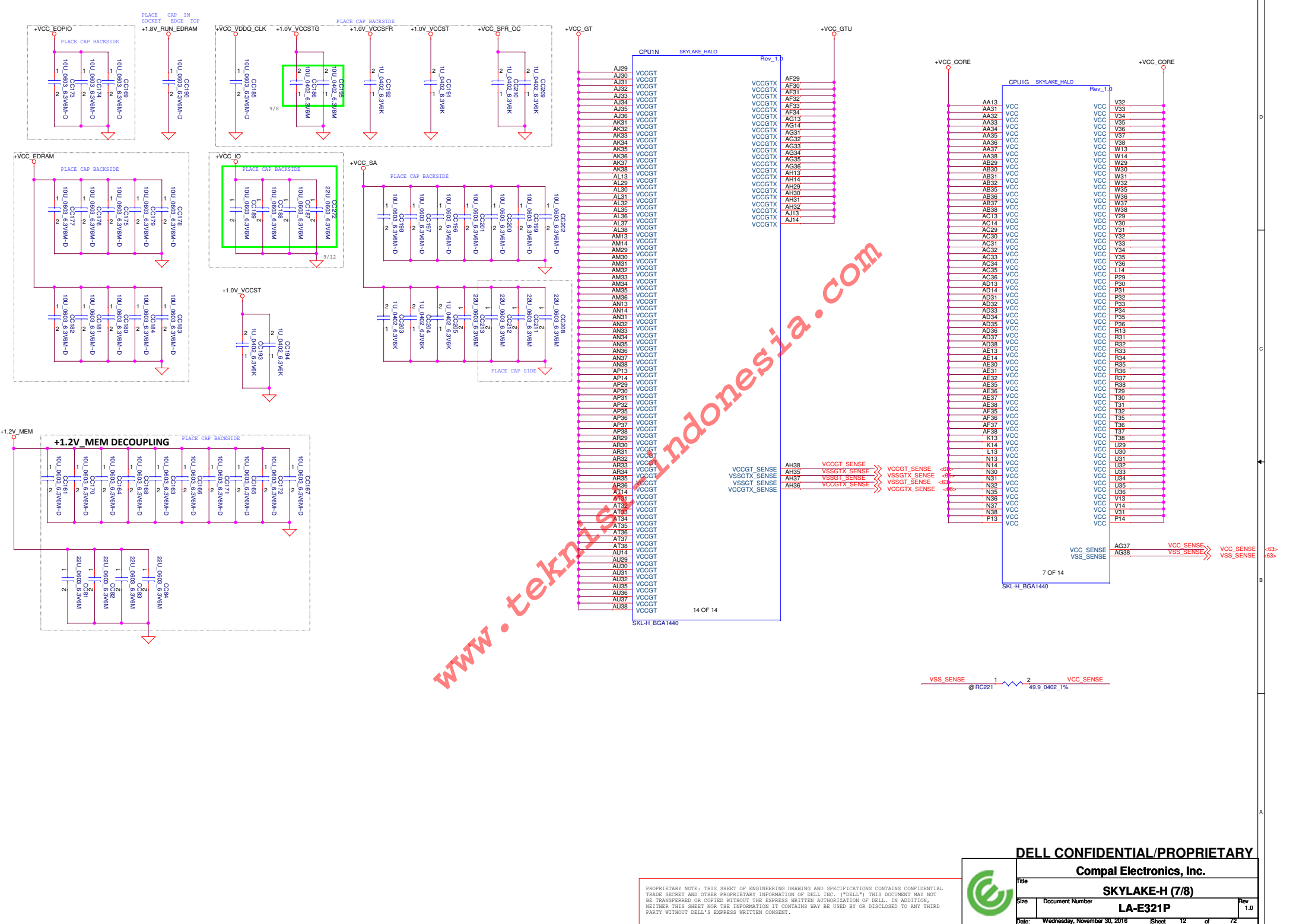
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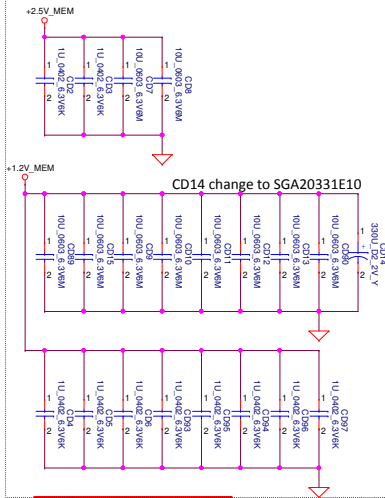
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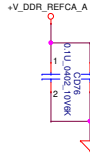
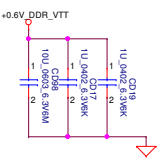
All VREF traces should have 10 mil trace width

JDIMM1 STD Type H=9.2

<8.15> DDR_A_DQS#0[0..7] <<>
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<8.15> DDR_A_DQ[0..63] <<>
<8.15> DDR_A_MA[0..13] <<>

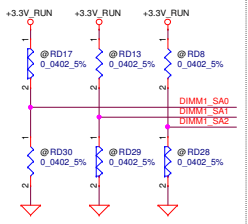


Layout Note:
Place near JDIMM1.258

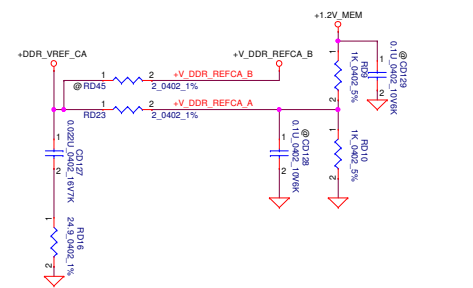
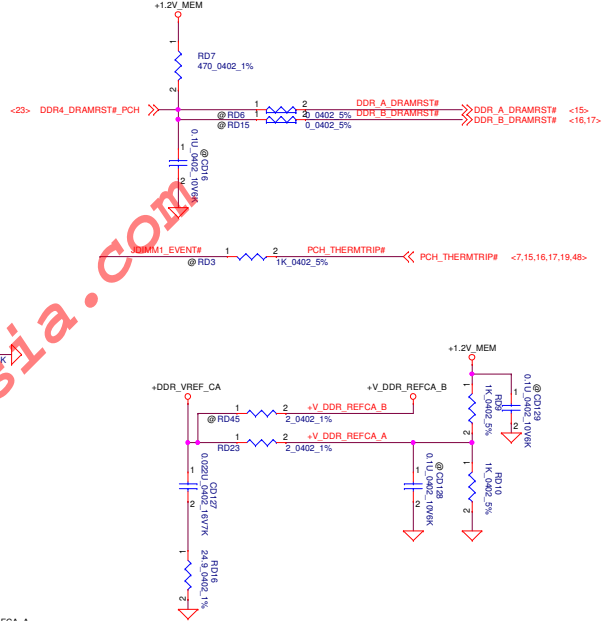
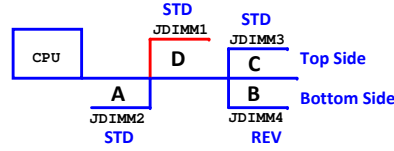
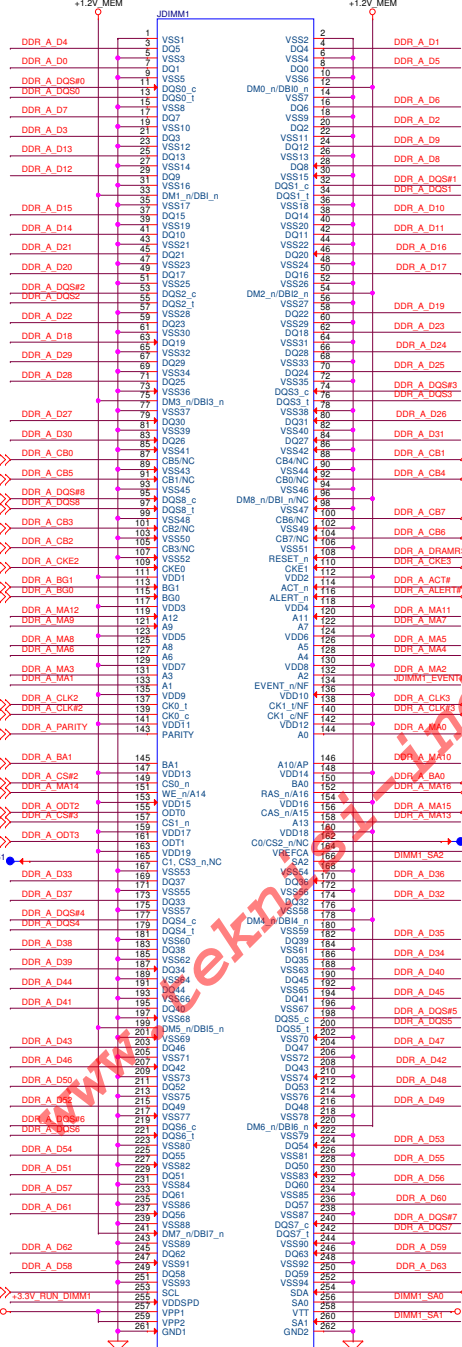


DIMM Select

	SA0	SA1	SA2
DIMM2	0	0	0
DIMM4	0	1	0
DIMM1	1	0	0
DIMM3	1	1	0



<7.15,16,17,23,43> DDR_XDP_WAN_SMBCLK <<>
<7.15,16,17,23,43> DDR_XDP_WAN_SMBDAT <<>
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DDR3L-SODIMM SLOT1

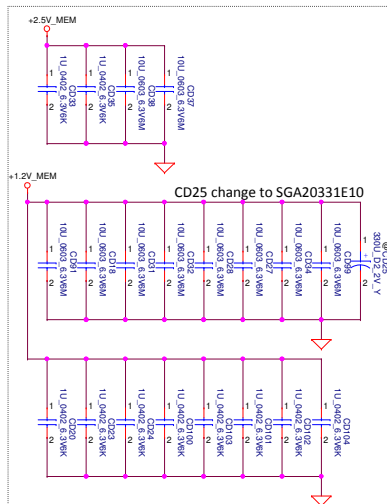
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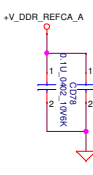
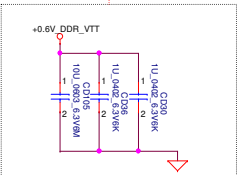
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JDIMM2 STD Type H=4

<8.14> DDR_A_DQS[0..7] <<>
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 <8.14> DDR_A_D[0..63] <<>
 <8.14> DDR_A_MA[0..13] <<>

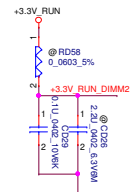
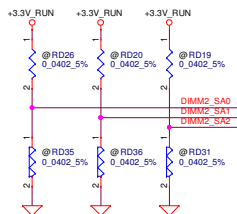


Layout Note:
Place near JDIMM2.258



DIMM Select

	SA0	SA1	SA2
* DIMM2	0	0	0
DIMM4	0	1	0
DIMM1	1	0	0
DIMM3	1	1	0



<7.14,16,17,23.43> DDR_XDP_WAN_SMBCLK <<>

+2.5V_MEM

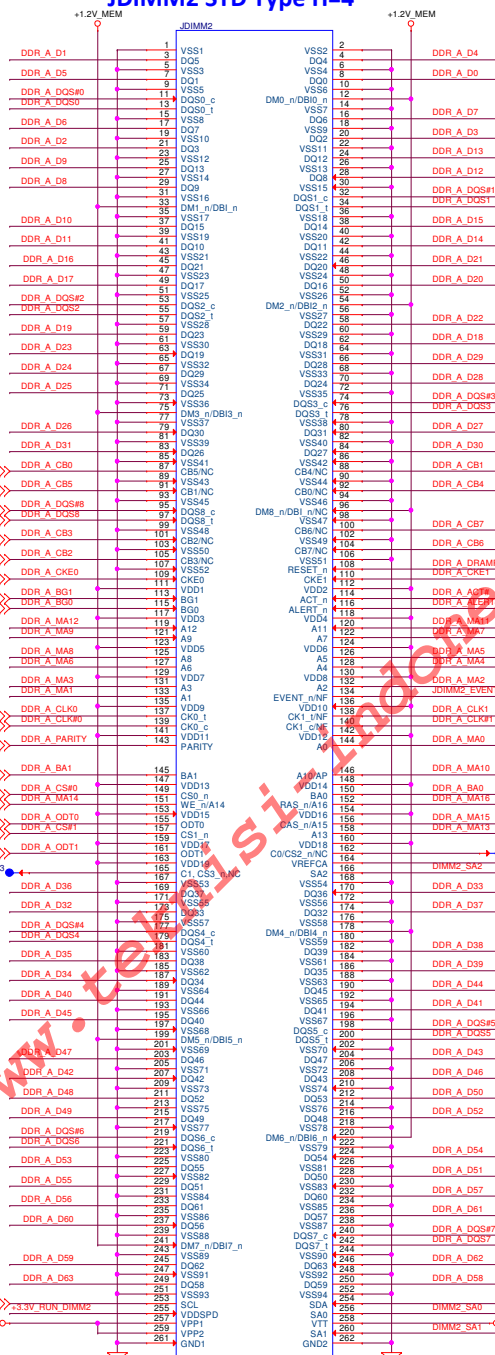
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 <8.14> DDR_A_CB5
 <8.14> DDR_A_DQS4
 <8.14> DDR_A_DQS8
 <8.14> DDR_A_CB3
 <8.14> DDR_A_CB2
 <8.14> DDR_A_CKE0
 <8.14> DDR_A_B01
 <8.14> DDR_A_B00

<8.14> DDR_A_BA1
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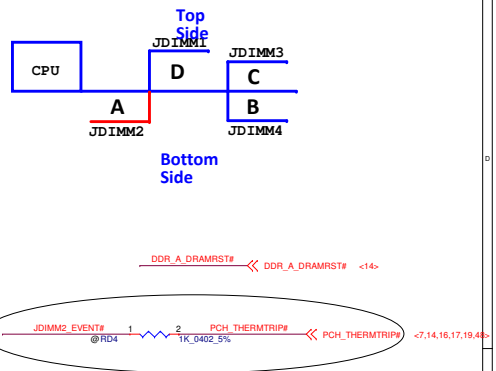
PAD-D @ T53

<7.14,16,17,23.43> DDR_XDP_WAN_SMBCLK <<>

+2.5V_MEM



LOTES_ADDR106-P005A
CONN@



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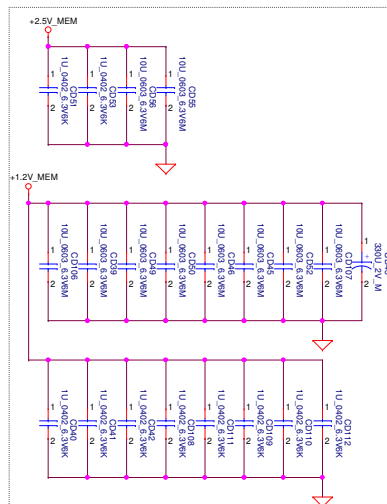
DDRIII-SODIMM SLOT2

LA-E321P

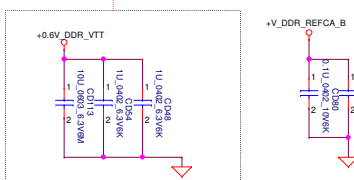
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JDIMM3 STD Type H=5.2

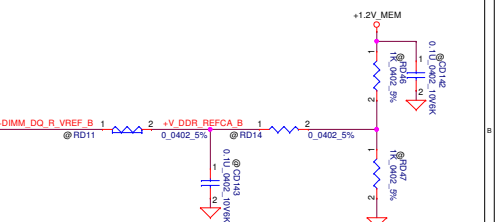
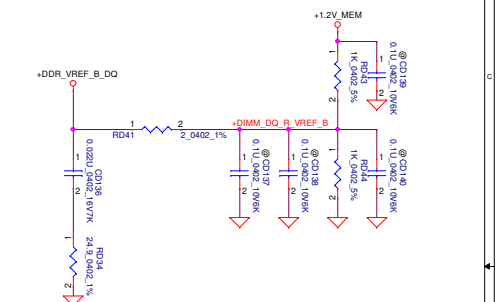
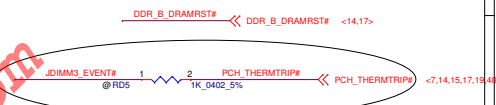
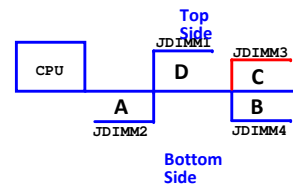
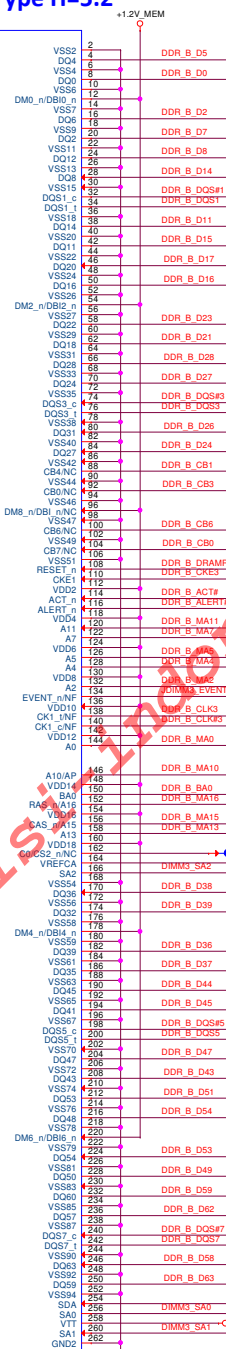
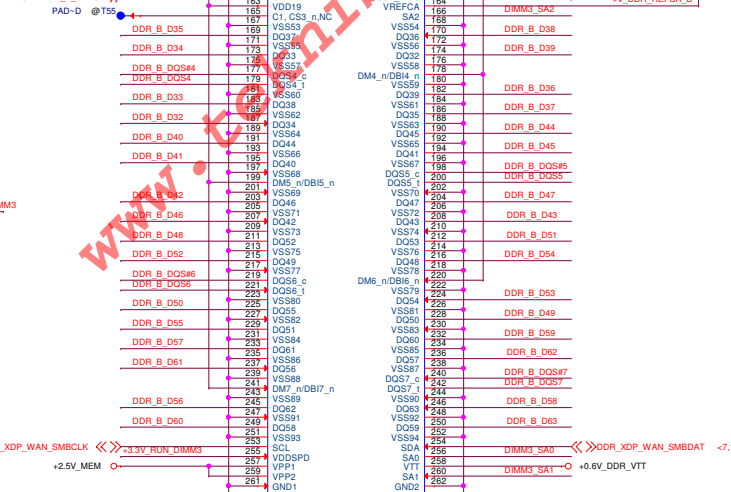
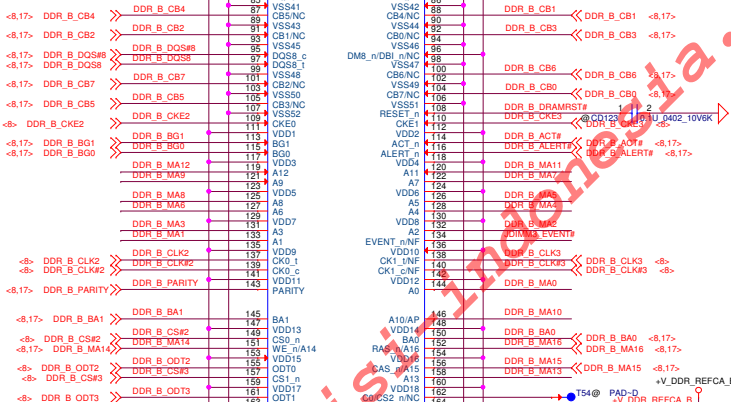
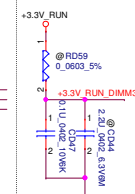
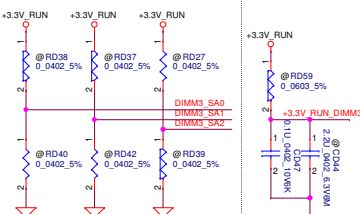


Layout Note:
Place near JDIMM3.258



DIMM Select

	SA0	SA1	SA2
DIMM2	0	0	0
DIMM4	0	1	0
DIMM1	1	0	0
* DIMM3	1	1	0



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DDRIII-SODIMM SLOT3

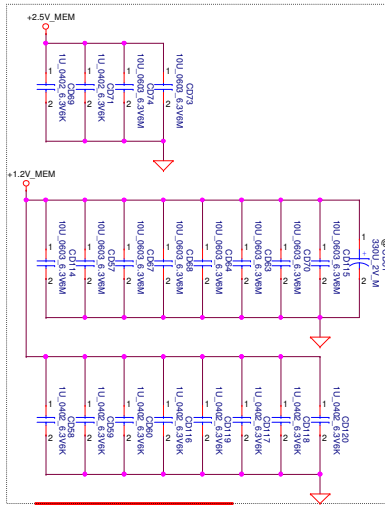
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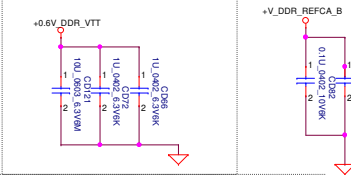


JDIMM Rev Type H=4

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 <8,16> DDR_B_DQS#0[7] <<>
 <8,16> DDR_B_DQ[0..63] <<>
 <8,16> DDR_B_MA[0..13] <<>



Layout Note:
Place near JDIMM4.258

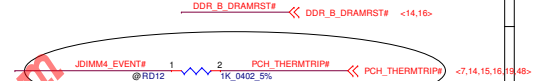
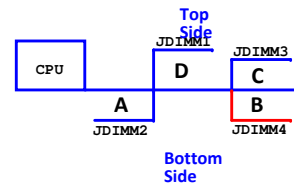
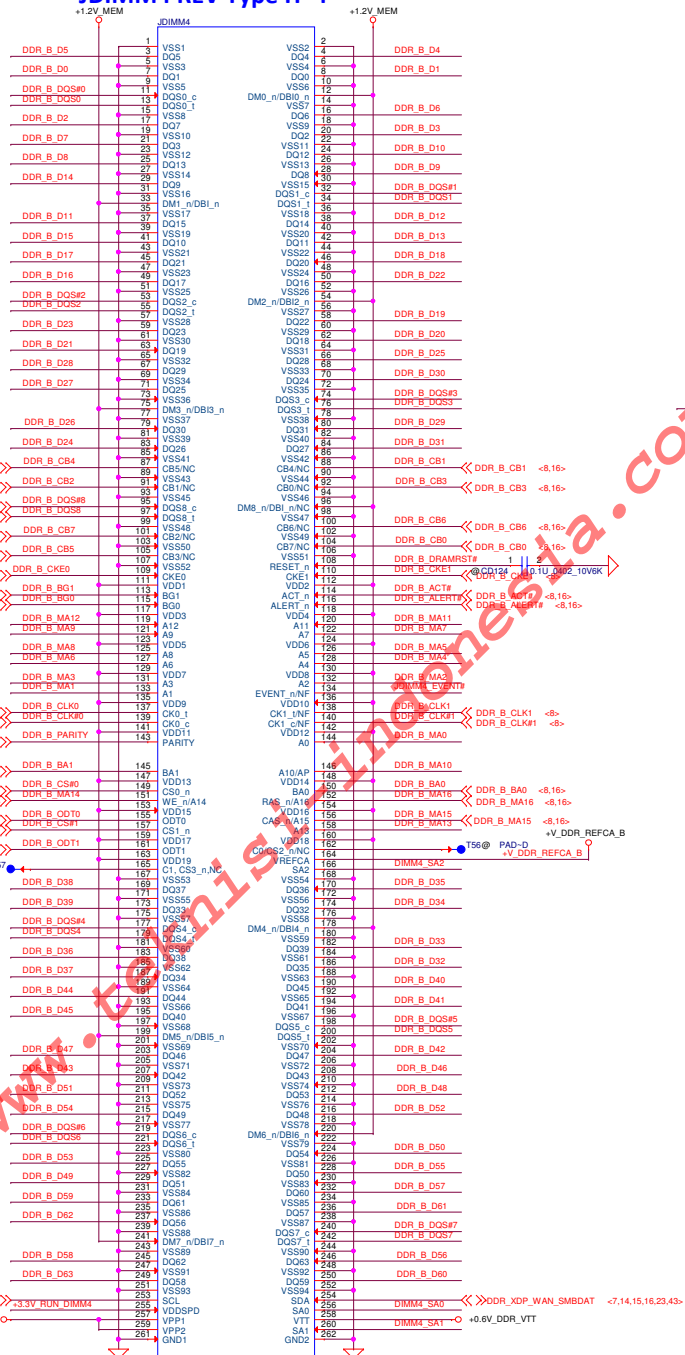


DIMM Select

	SA0	SA1	SA2
DIMM2	0	0	0
DIMM4	0	1	0
DIMM1	1	0	0
DIMM3	1	1	0

<7,14,15,16,23,43> DDR_XDP_WAN_SMBCLK <<>

+2.5V MEM



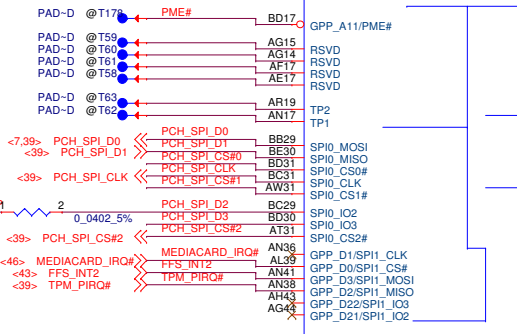
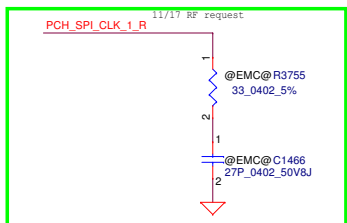
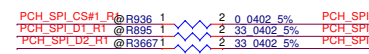
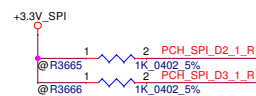
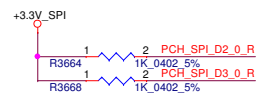
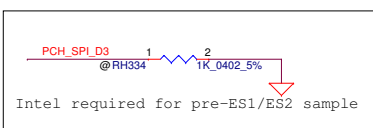
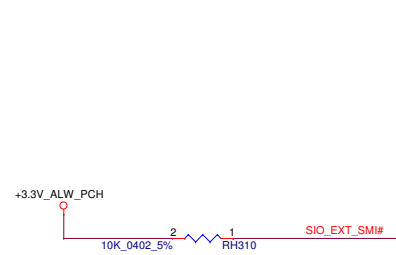
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DDR3II-SODIMM SLOT4

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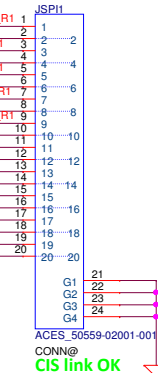
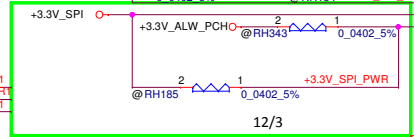
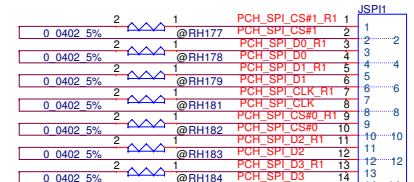
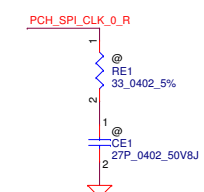
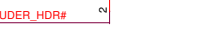
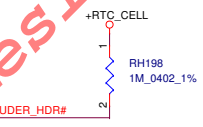
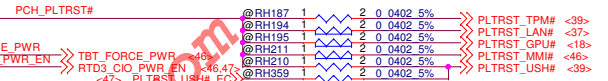
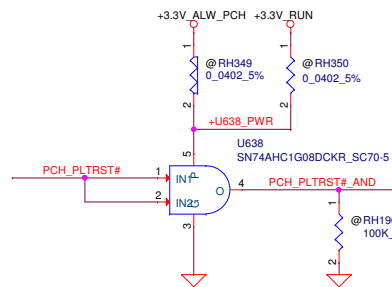
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200 MIL SO8 16MB Flash ROM

200 MIL SO8 4MB Flash ROM

CIS LINK OK



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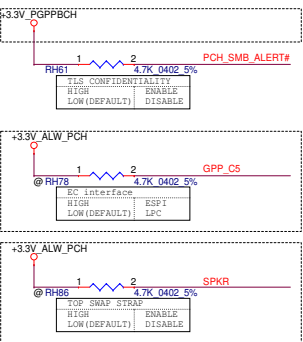
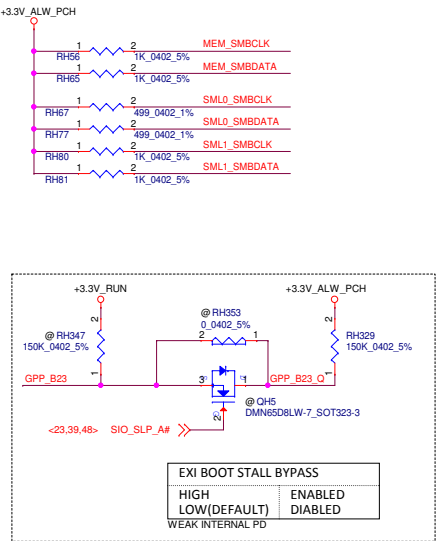
SKYLAKE PCH-H (4/9)

LA-E321P

Rev 1.0

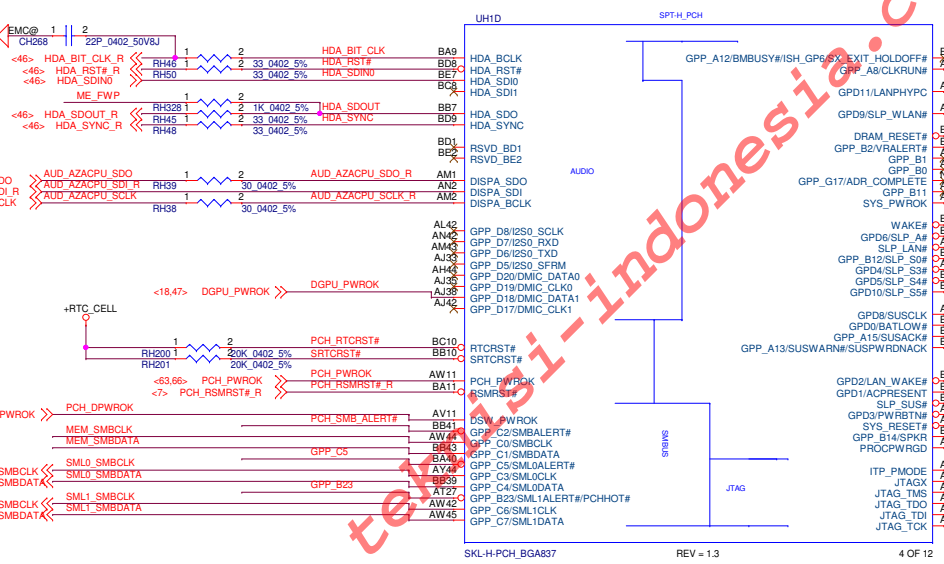
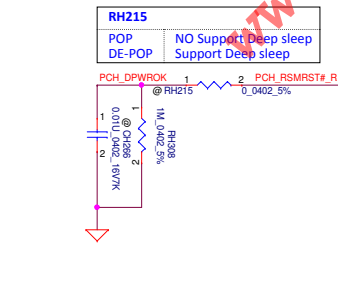
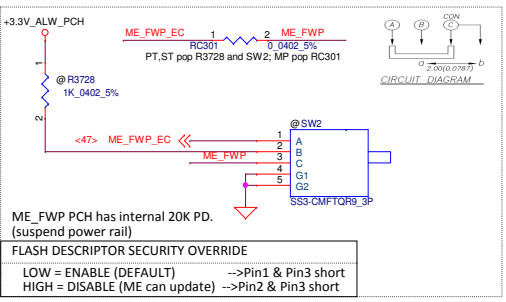
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Service Mode Switch:

Add a switch to ME_FWP signal to unlock the ME region and allow the entire region of the SPI flash to be updated using FPT.

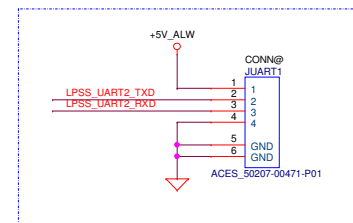
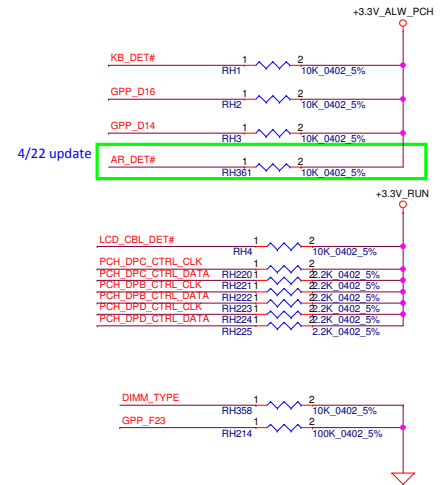
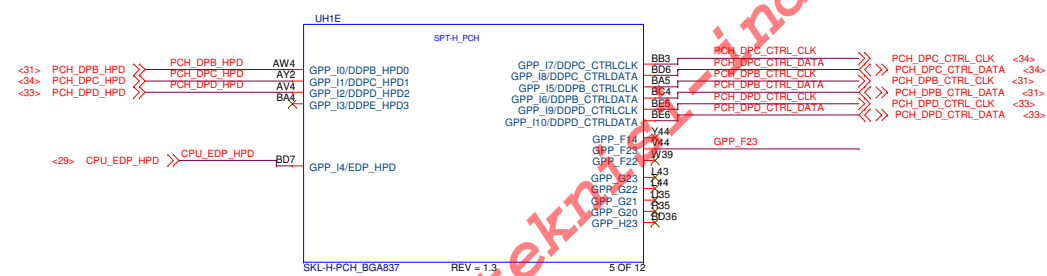
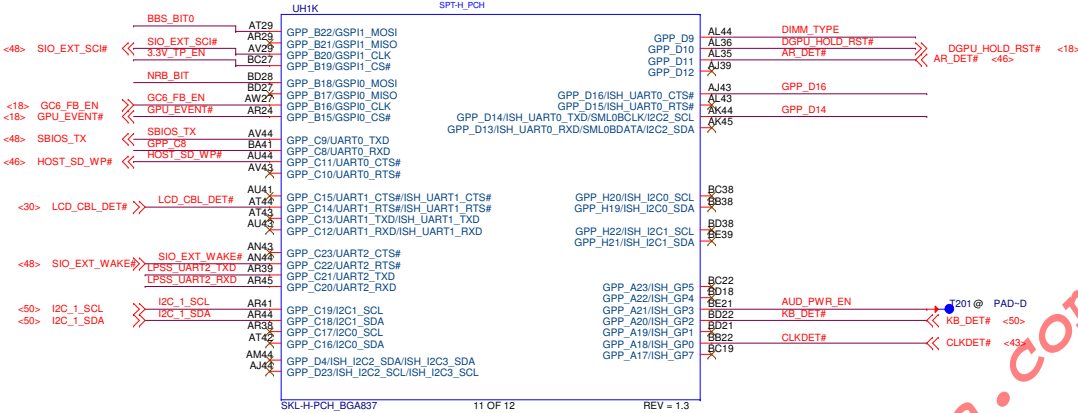
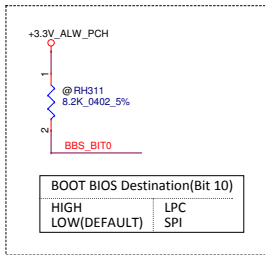
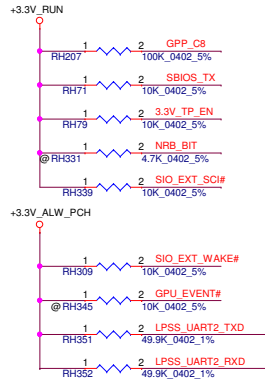


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SKYLAKE PCH-H (5/9)	
LA-E321P	
Date:	Thursday, December 08, 2016
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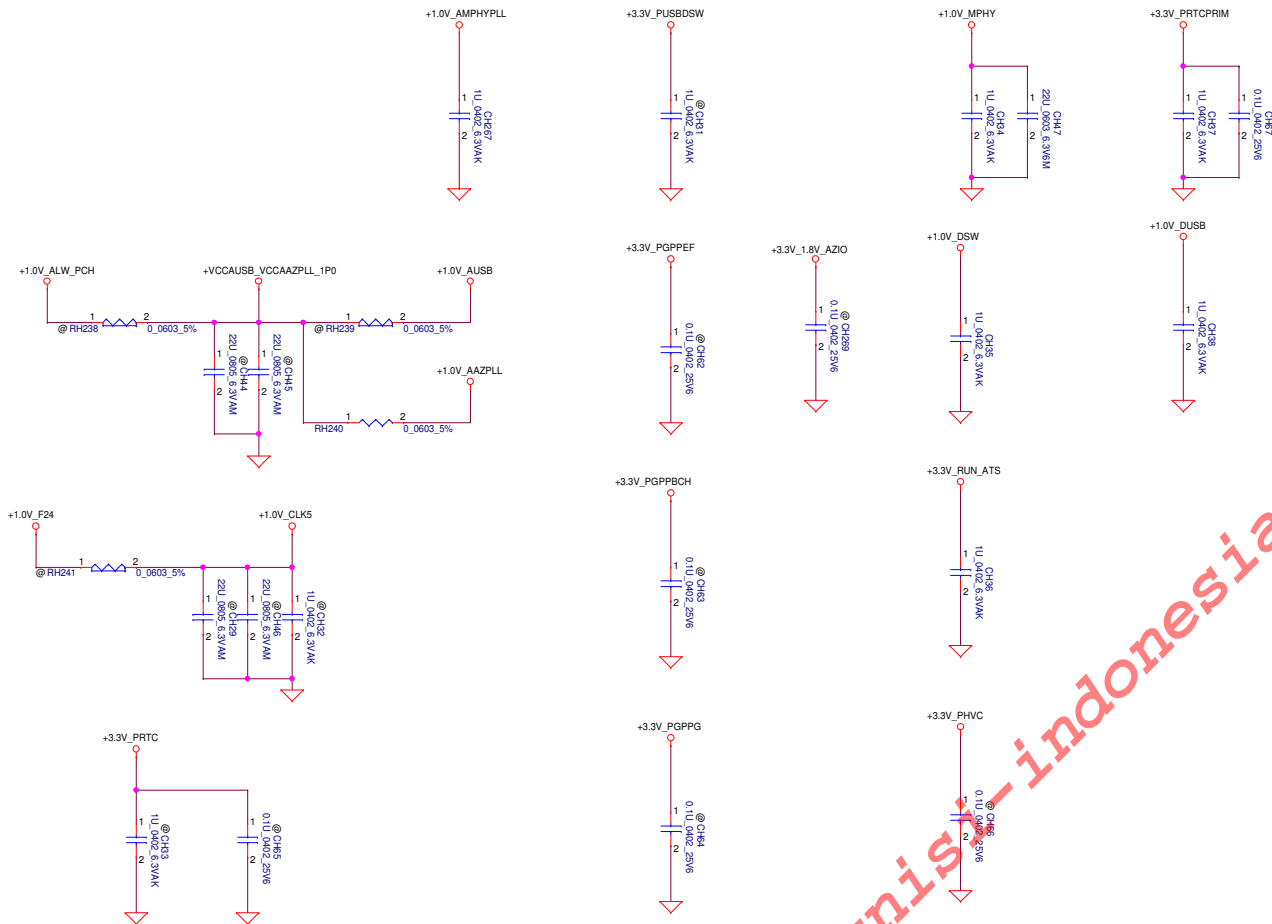
SKYLAKE PCH-H (6/9)

LA-E321P

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LA-E321P		LA-E321P		1.0
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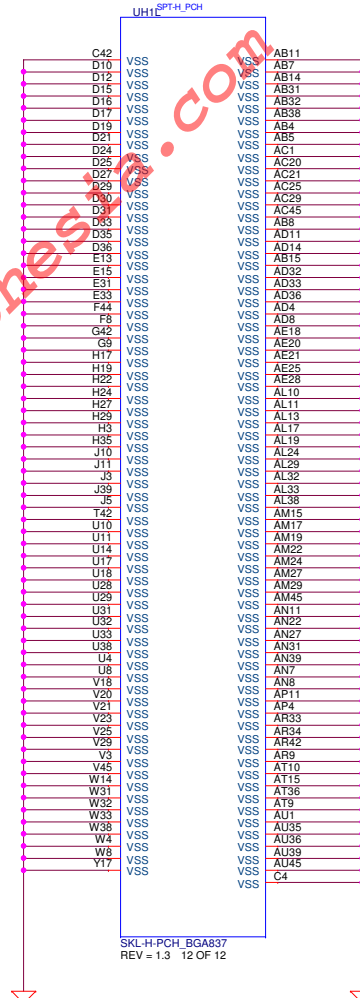
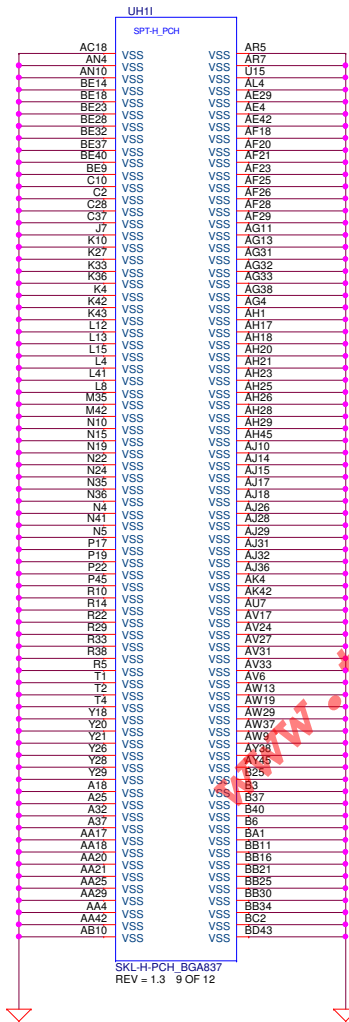
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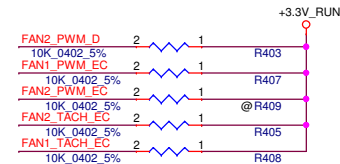
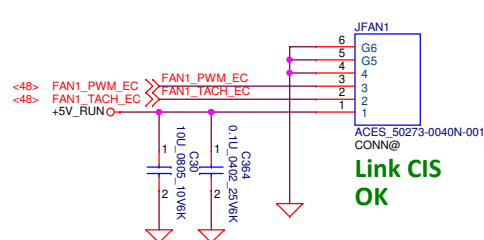
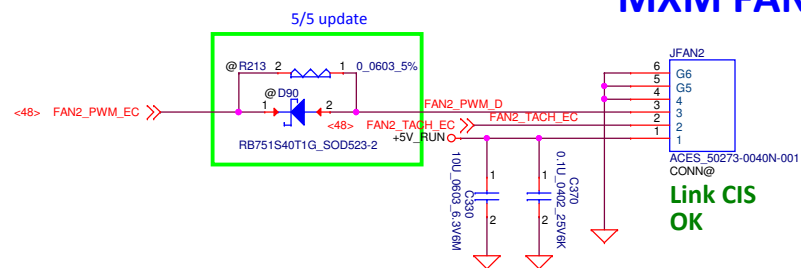
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SKYLAKE PCH-H (9/9)			
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MXM FAN

CPU FAN



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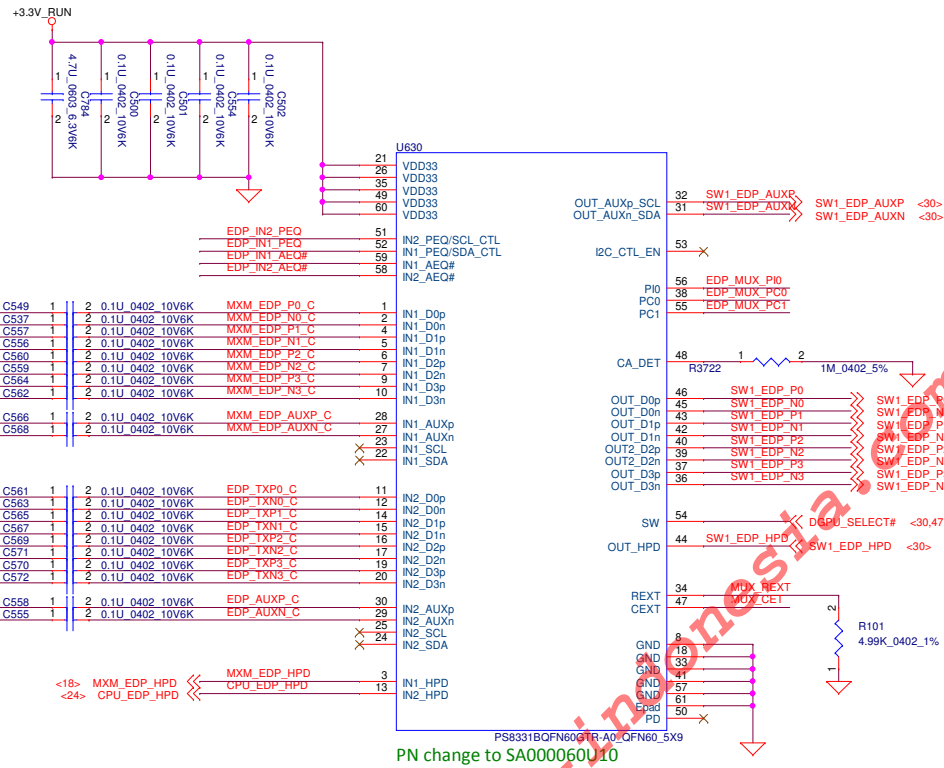


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Size	Document Number	LA-E321P	
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		Rev	1.0

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MXM

CPU

eDP
Conn

DGPU_SELECT#; 0: MXM ; 1: i-GPU

SW	Input
H	IN2
L (Default)	IN1

INy_PEQ = Programmable input equalization levels
L: default, LEQ, compensate channel loss up to 11.5dB @ HBR2
H: HEQ, compensate channel loss up to 14.5dB @ HBR2
M: LLEQ, compensate channel loss up to 8.5dB @ HBR2

INy_AEQ# = Automatic EQ disable
L: Automatic EQ enable (default)
H: Automatic EQ disable

PI0 = Auto test enable
L: Auto test disable & input offset cancellation enable (default)
H: Auto test enable & input offset cancellation enable
M: Auto test disable & input offset cancellation disable

PC0 = AUX interception disable
L: AUX interception enable, driver configuration is set by link training (default)
H: AUX interception disable, driver output with fixed 800mV and 0dB
M: AUX interception disable, driver output with fixed 400mV and 0dB

PC1 = Output swing adjustment
L: default
H: +20%
M: -16.7%

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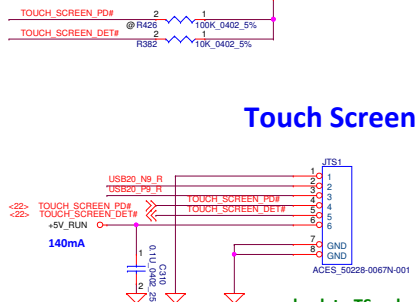
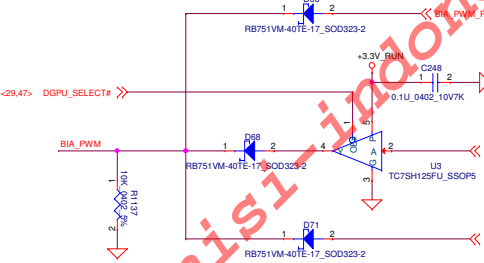
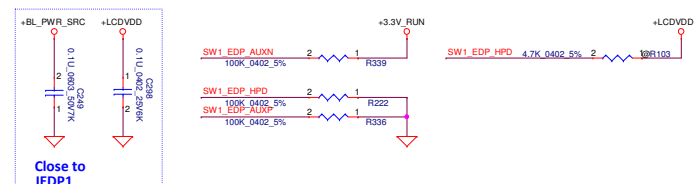
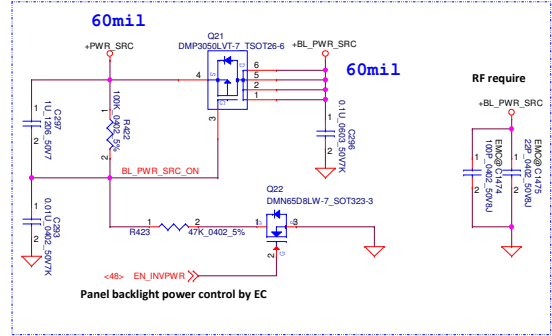
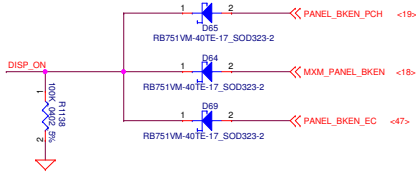
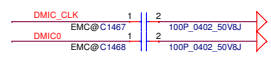
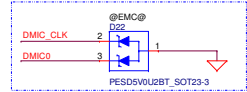
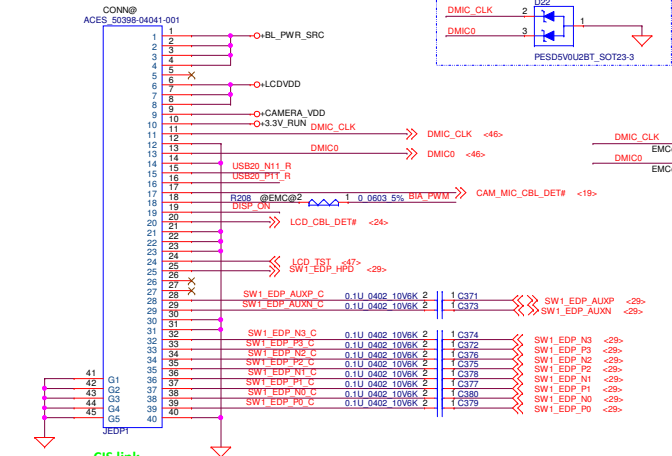
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Size	Document Number		Rev 1.0
LA-E321P			
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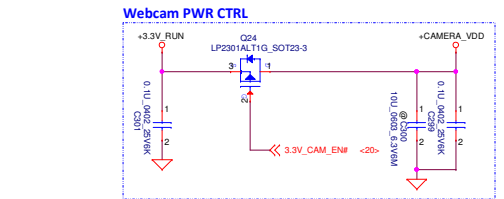
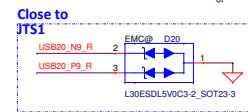
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5/5 update

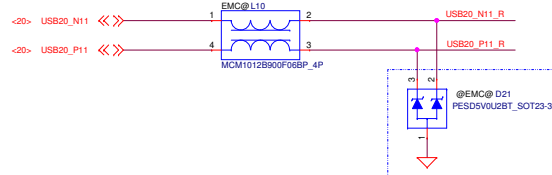


Touch Screen

back to TS only

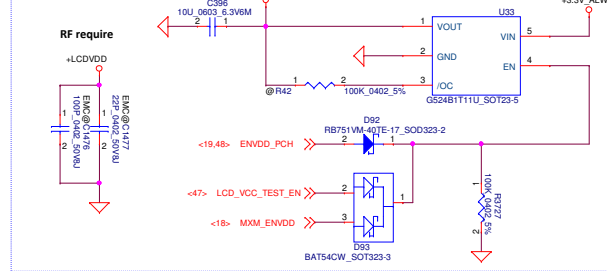


EMC request change main source to SM070003200



Close to JEDP1

LCD Power



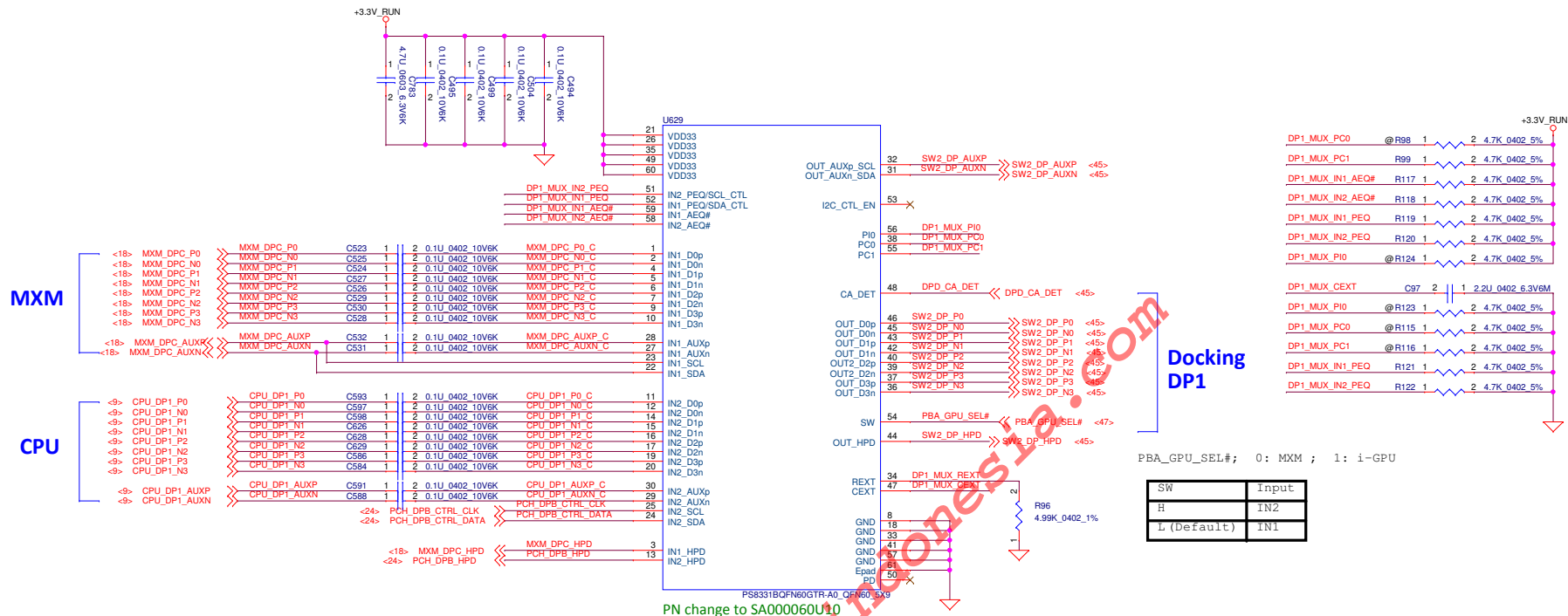
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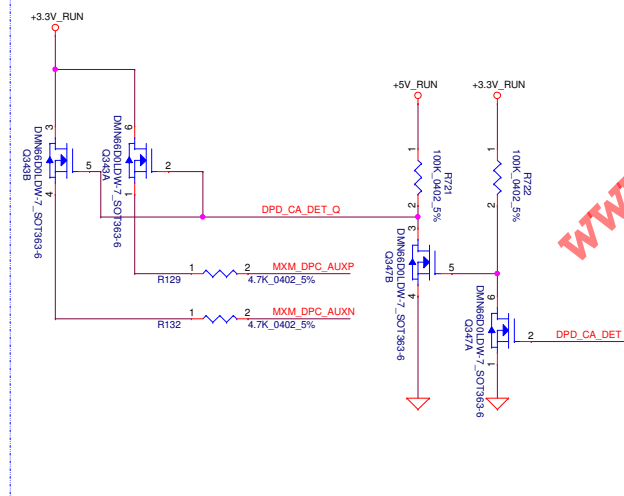


Docking DP1

PBA_GPU_SEL#; 0: MXM ; 1: i-GPU

SW	Input
H	IN2
L (Default)	IN1

DOCK DPD (PORT1) DDC-before PS8331



INy_PEQ = Programmable input equalization levels
 L: default, LEQ, compensate channel loss up to 11.5dB @ HBR2
 H: HEQ, compensate channel loss up to 14.5dB @ HBR2
 M: LLEQ, compensate channel loss up to 8.5dB @ HBR2

INy_AEQ# = Automatic EQ disable
 L: Automatic EQ enable (default)
 H: Automatic EQ disable

PI0 = Auto test enable
 L: Auto test disable & input offset cancellation enable (default)
 H: Auto test enable & input offset cancellation enable
 M: Auto test disable & input offset cancellation disable

PC0 = AUX interception disable
 L: AUX interception enable, driver configuration is set by link training (default)
 H: AUX interception disable, driver output with fixed 800mV and 0dB
 M: AUX interception disable, driver output with fixed 400mV and 0dB

PC1 = Output swing adjustment
 L: default
 H: +20%
 M: -16.7%

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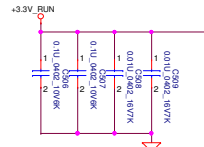
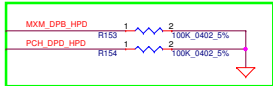
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MXM/CPU MUX(P8331)

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11/09 update



MXM

<18> MXM DPB P0
<18> MXM DPB N0
<18> MXM DPB P1
<18> MXM DPB N1
<18> MXM DPB P2
<18> MXM DPB N2
<18> MXM DPB P3
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<18> MXM DPB AUXP
<18> MXM DPB AUXN

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MXM DPB N0 C
MXM DPB P1 C
MXM DPB N1 C
MXM DPB P2 C
MXM DPB N2 C
MXM DPB P3 C
MXM DPB N3 C
MXM DPB AUXP C
MXM DPB AUXN C

C587 1 2 0.1U 0402 10V8K
C588 1 2 0.1U 0402 10V8K
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C595 1 2 0.1U 0402 10V8K
C596 1 2 0.1U 0402 10V8K
C597 1 2 0.1U 0402 10V8K

MXM DPB P0 C
MXM DPB N0 C
MXM DPB P1 C
MXM DPB N1 C
MXM DPB P2 C
MXM DPB N2 C
MXM DPB P3 C
MXM DPB N3 C
MXM DPB AUXP C
MXM DPB AUXN C

B4 DA0_P
A4 DA0_N
B5 DA1_P
A5 DA1_N
B6 DA2_P
A6 DA2_N
B7 DA3_P
A7 DA3_N
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J9 AUXA_N
H8 DDCCLK_A
J8 DDCDAT_A
H7 HPDA

PORT A
PORT B
PORT C

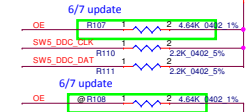
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DC1_P
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DC2_P
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DC3_P
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H1 SW5_DP_AUXN
J3 SW5_DDC_CLK
J7 SW5_DDC_DAT
J1 SW5_DP_TPD

SW5_DP_P0
SW5_DP_N0
SW5_DP_P1
SW5_DP_N1
SW5_DP_P2
SW5_DP_N2
SW5_DP_P3
SW5_DP_N3
SW5_DP_AUXP
SW5_DP_AUXN
SW5_DDC_CLK
SW5_DDC_DAT
SW5_DP_HPD

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7/7 update
Swap Lane2 N/P for incorrect symbol
9/13 Update correct symbol

mDP



OE	Output enable
H	Normal Operation
L (Default)	Standby Mode

DP2_GPU_SEL#;
0: MXM ; 1: i-GPU

DX_SEL	Input
H	Port B
L (Default)	Port A

SW5_DP_CA_DET;
0: DP; 1: HDMI

AUX_SEL	To/From
H	DDC
L (Default)	AUX

CPU

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<9> CPU DP3 N0
<9> CPU DP3 P1
<9> CPU DP3 N1
<9> CPU DP3 P2
<9> CPU DP3 N2
<9> CPU DP3 P3
<9> CPU DP3 N3
<9> CPU DP3 AUXP
<9> CPU DP3 AUXN

CPU DP3 P0
CPU DP3 N0
CPU DP3 P1
CPU DP3 N1
CPU DP3 P2
CPU DP3 N2
CPU DP3 P3
CPU DP3 N3
CPU DP3 AUXP
CPU DP3 AUXN

C1448 1 2 0.1U 0402 10V8K
C1450 1 2 0.1U 0402 10V8K
C1453 1 2 0.1U 0402 10V8K
C1451 1 2 0.1U 0402 10V8K
C1449 1 2 0.1U 0402 10V8K
C1454 1 2 0.1U 0402 10V8K
C1455 1 2 0.1U 0402 10V8K
C1452 1 2 0.1U 0402 10V8K
C1447 1 2 0.1U 0402 10V8K
C1446 1 2 0.1U 0402 10V8K

CPU DP3 P0 C
CPU DP3 N0 C
CPU DP3 P1 C
CPU DP3 N1 C
CPU DP3 P2 C
CPU DP3 N2 C
CPU DP3 P3 C
CPU DP3 N3 C
CPU DP3 AUXP C
CPU DP3 AUXN C

B8 DB0_P
B7 DB0_N
D8 DB1_P
E8 DB1_N
F8 DB2_P
G8 DB2_N
H8 DB3_P
J8 DB3_N
H6 AUXB_P
J6 AUXB_N
H5 DDCCLK_B
J5 DDCDAT_B
H4 HPDB

PORT A
PORT B
PORT C

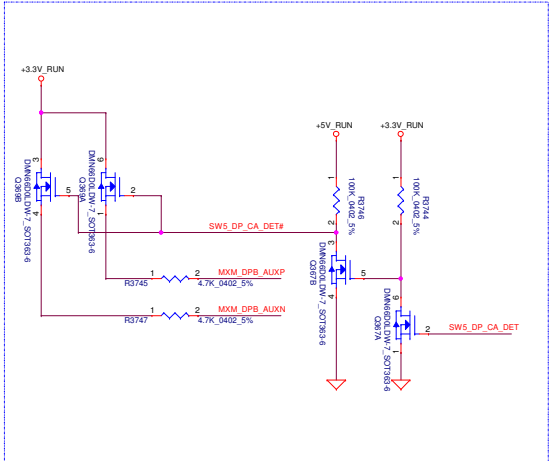
DC0_P
DC0_N
DC1_P
DC1_N
DC2_P
DC2_N
DC3_P
DC3_N
H2 SW5_DP_AUXP
H1 SW5_DP_AUXN
J3 SW5_DDC_CLK
J7 SW5_DDC_DAT
J1 SW5_DP_TPD

SW5_DP_P0
SW5_DP_N0
SW5_DP_P1
SW5_DP_N1
SW5_DP_P2
SW5_DP_N2
SW5_DP_P3
SW5_DP_N3
SW5_DP_AUXP
SW5_DP_AUXN
SW5_DDC_CLK
SW5_DDC_DAT
SW5_DP_HPD

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7/7 update
Swap Lane2 N/P for incorrect symbol
9/13 Update correct symbol

mDP



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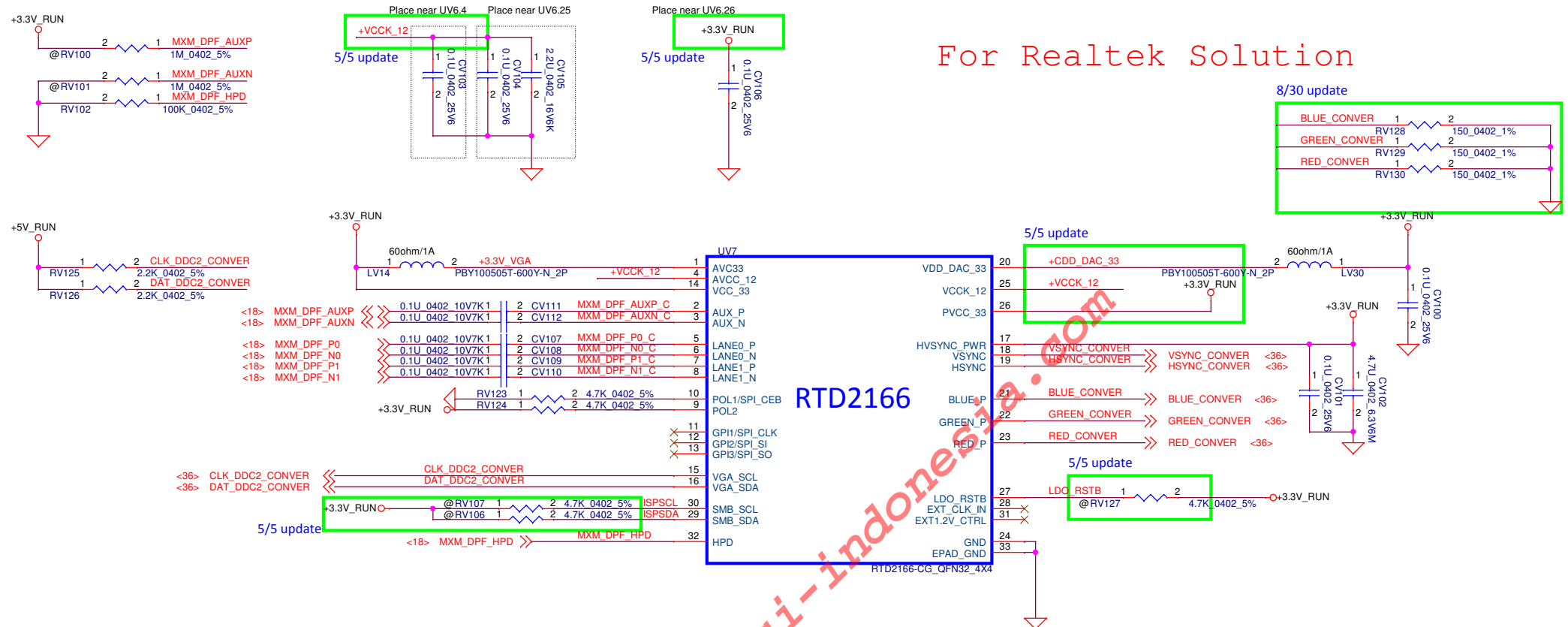
Compal Electronics, Inc.

P33-mDP MB DP1.3 MUX (HD3SS214)

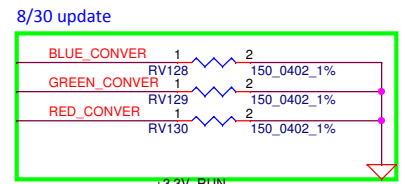
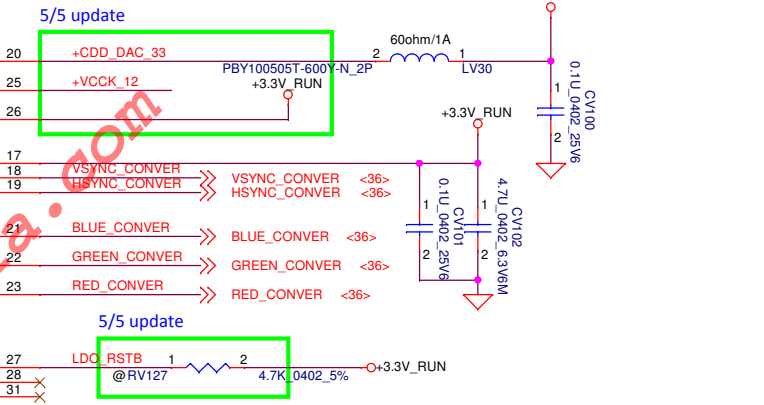
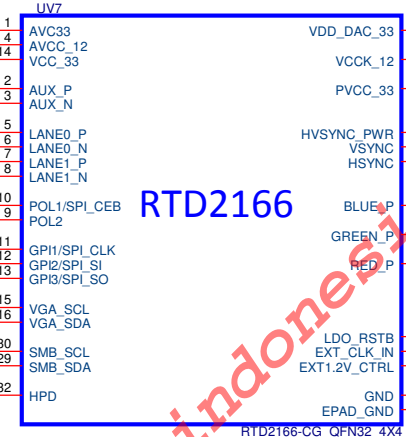
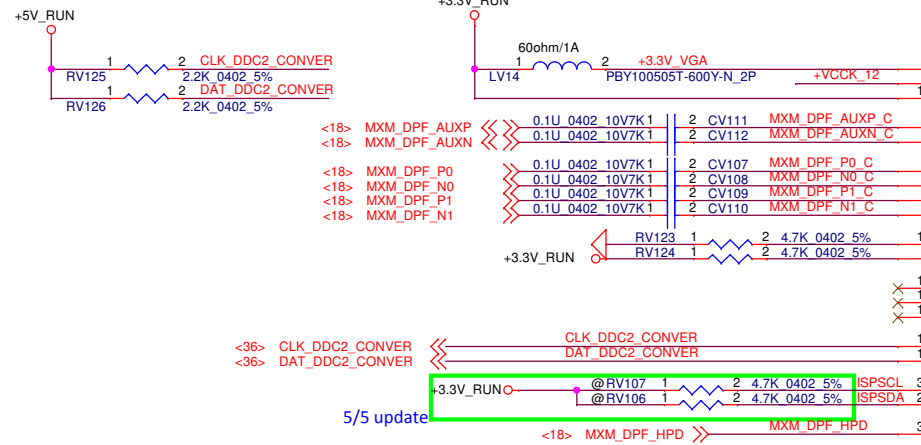
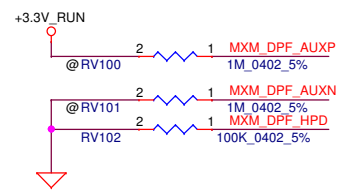
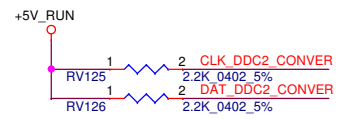
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For Realtek Solution



Operation Mode Table			
		POL1(P10)	
POL2 (P9)	0	X	X
	1	ROM	Flash

Security Classification		Compal Secret Data		Compal Electronics, Inc.	
Issued Date	2016/01/01	Deciphered Date	2017/01/01	Title	DP to VGA
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				Date:	Wednesday, November 30, 2016
				Sheet	35 of 72

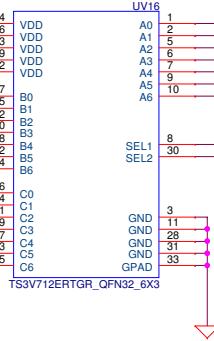
From MXM
From convertor

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<18> GREEN_MXM
<18> BLUE_MXM
<18> HSYNC_MXM
<18> VSYNC_MXM
<18> DAT_DDC2_MXM
<18> CLK_DDC2_MXM

<35> RED_CONVERTER
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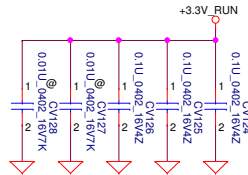
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GREEN_MXM
BLUE_MXM
HSYNC_MXM
VSYNC_MXM
DAT_DDC2_MXM
CLK_DDC2_MXM

RED_CONVERTER
GREEN_CONVERTER
BLUE_CONVERTER
HSYNC_CONVERTER
VSYNC_CONVERTER
DAT_DDC2_CONVERTER
CLK_DDC2_CONVERTER

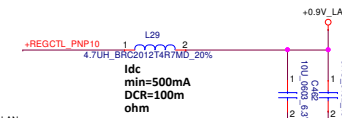
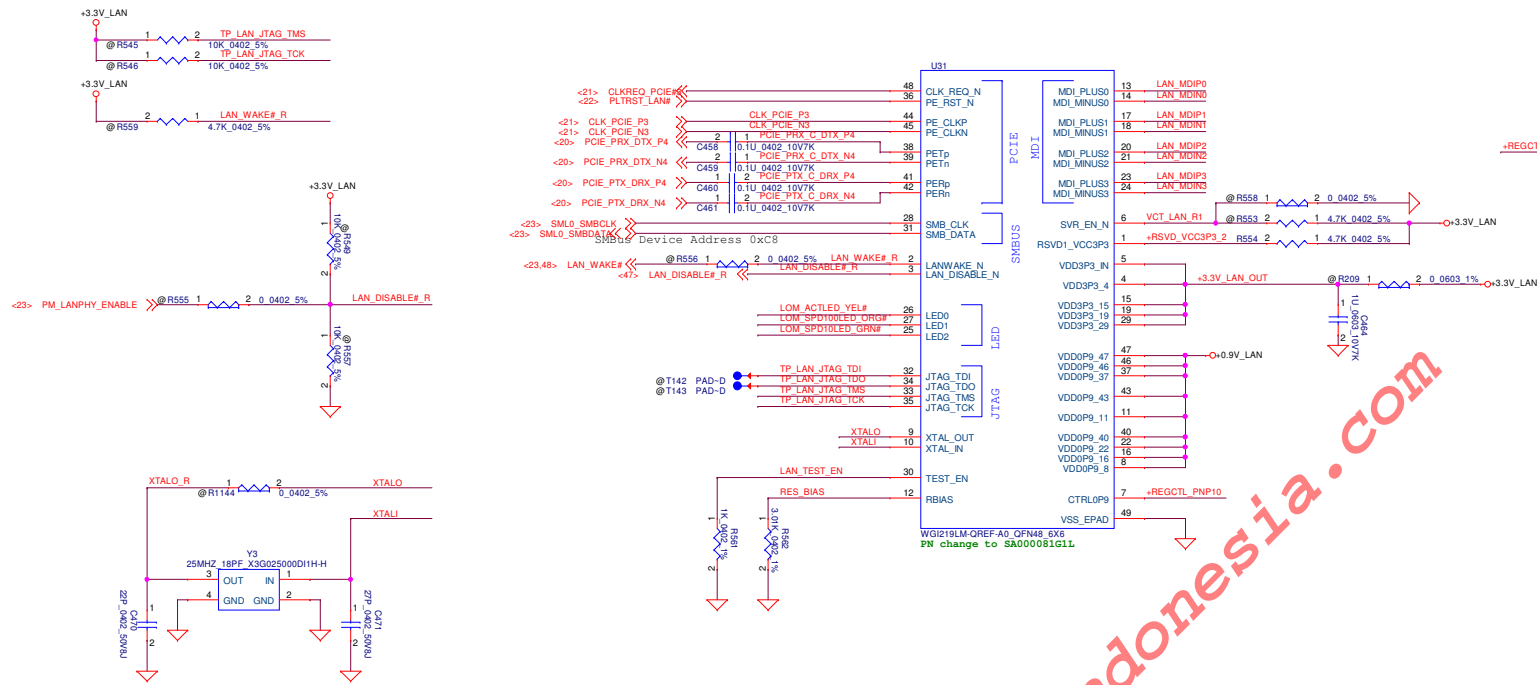


To VGA DOCK

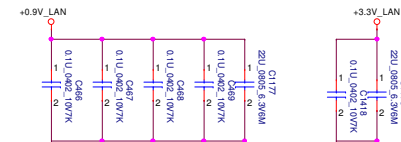
MXM_SELECT	Chanel	Source
0	A=B1	MXM_VGA
1	A=B2	CONVERTER



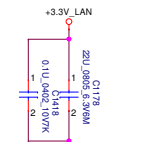
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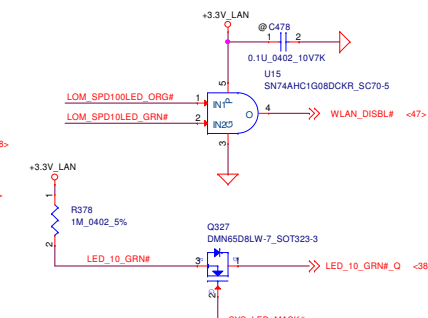
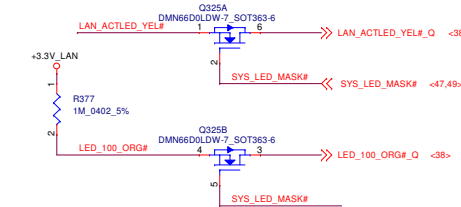
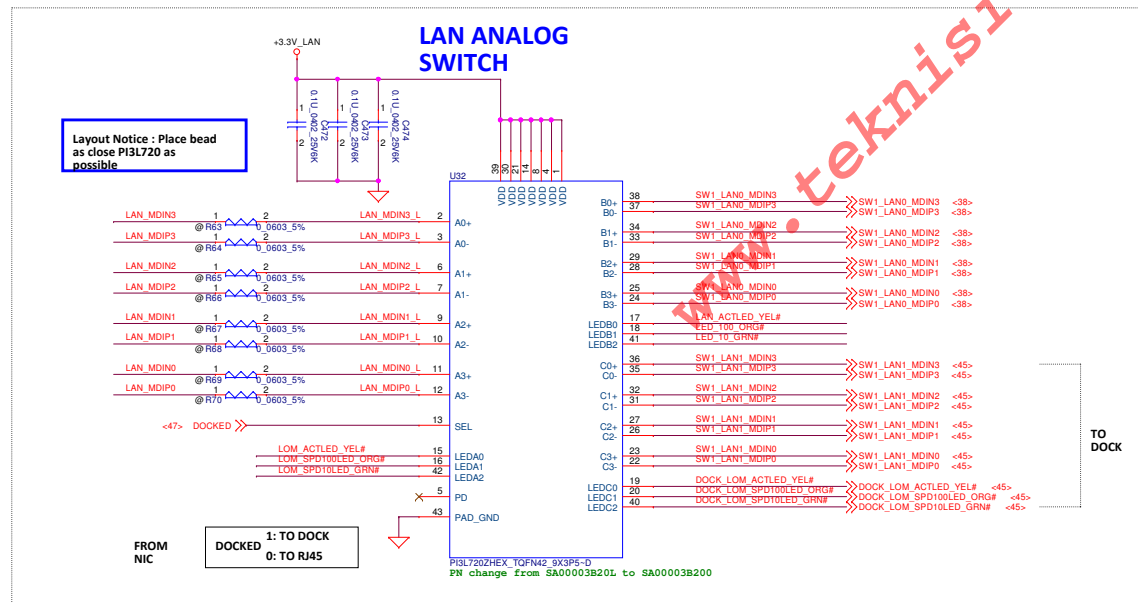
Place C462, C463 and L29 close to U31



Note: +1.0V_LAN will work at 0.95V to 1.15V



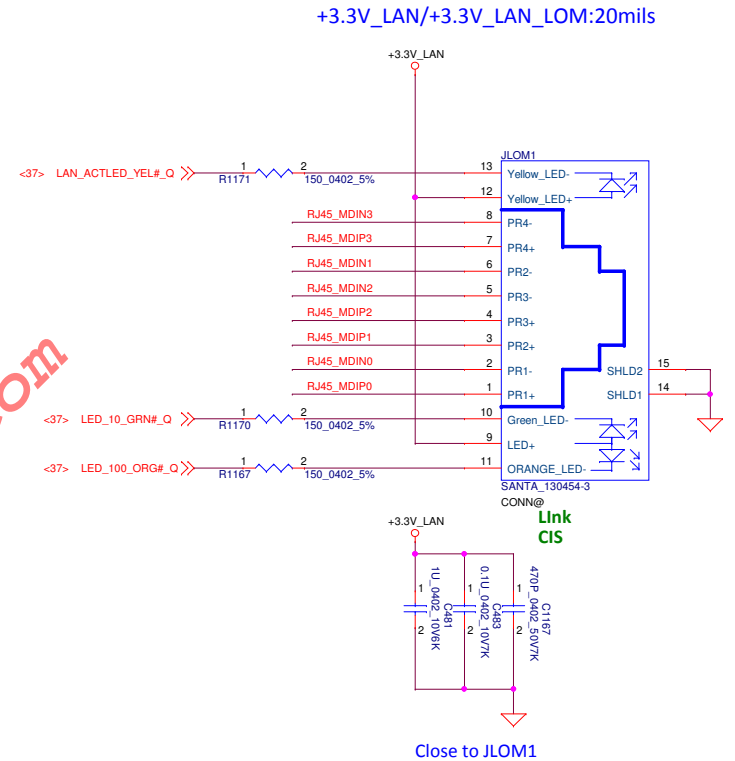
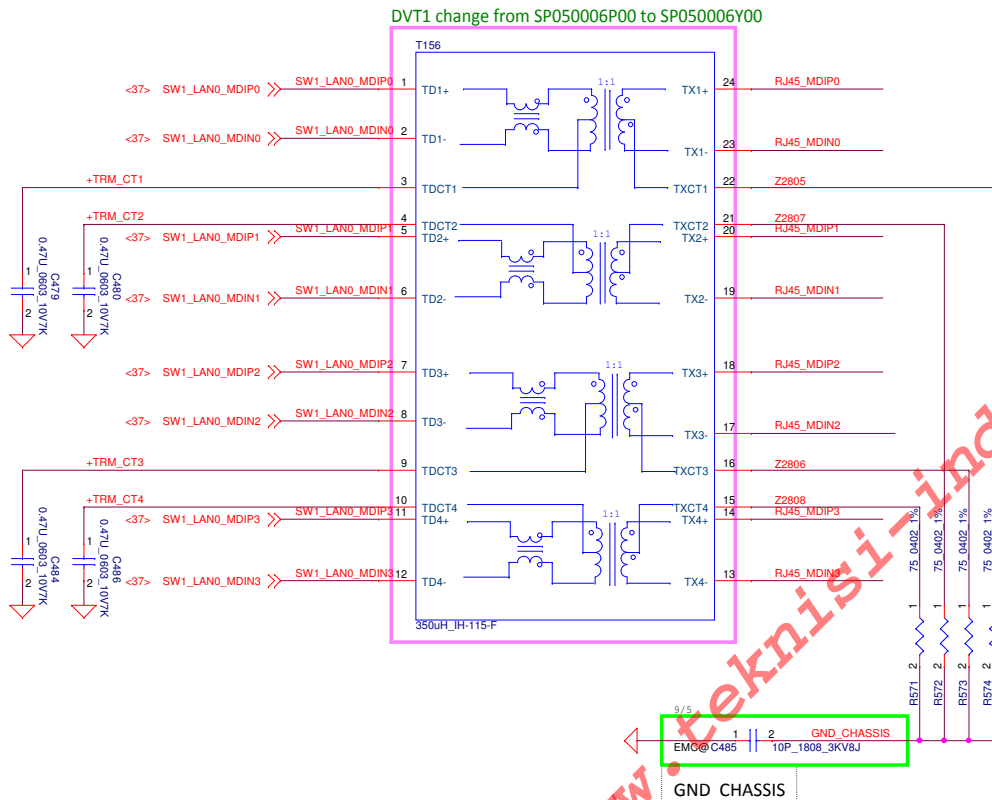
Place C1178 close to pin5



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LAN/LAN SW			
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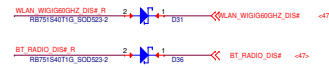
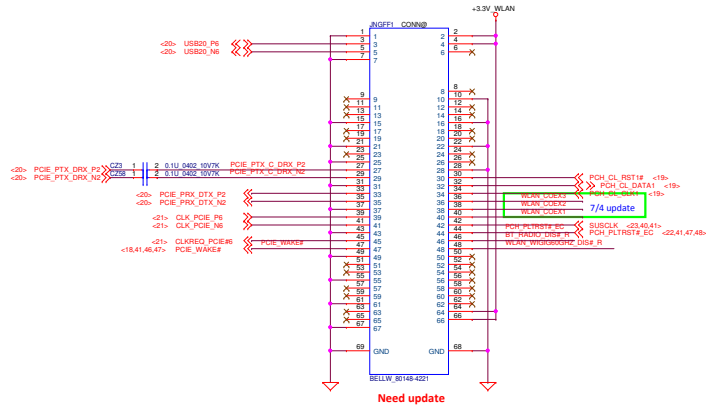
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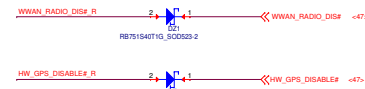
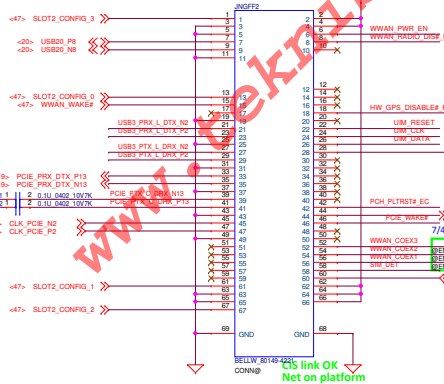
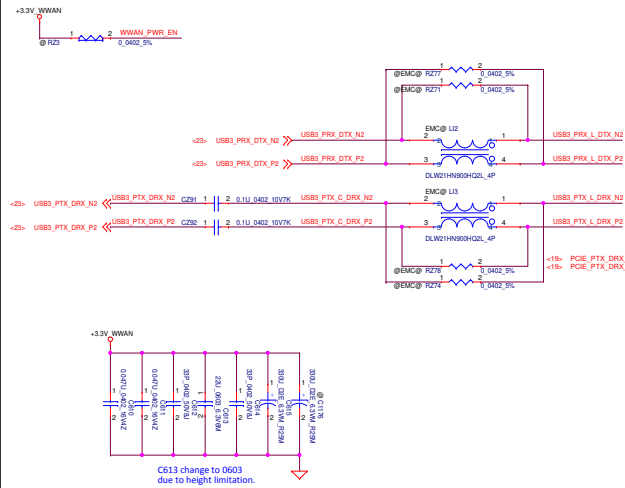
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RJ45			
Size	Document Number	LA-E321P	Rev 1.0
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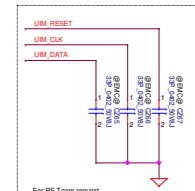
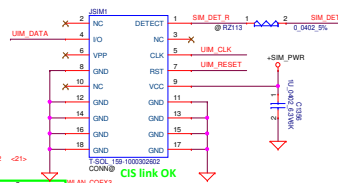
WLAN/BT NGFF slot_1 Key A



WWAN/LTE/HCA/Cache NGFF slot_2 Key B



SIM Card Push-Push



STATE #	CONFIG_0	CONFIG_1	CONFIG_2	CONFIG_3	Module Type
0	0	0	0	0	SSD-SATA
8	1	0	0	0	WWAN
14	1	0	1	1	HCA-PCIE
15	1	1	1	1	Cache

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M.2 Card-1/2

Document Number

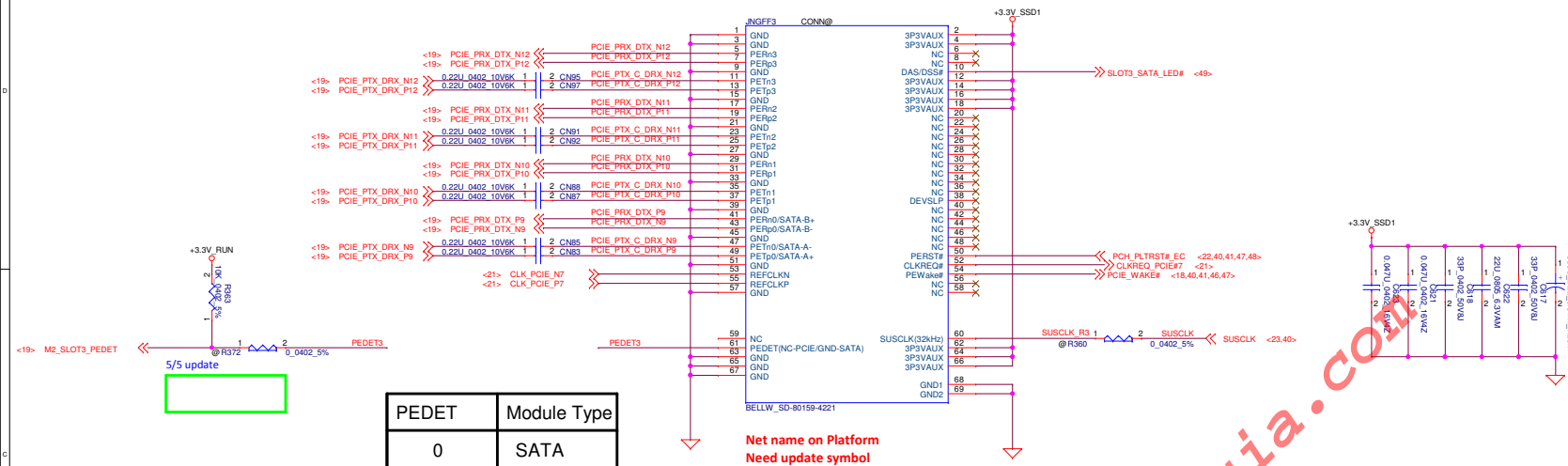
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Monday, December 14, 2015

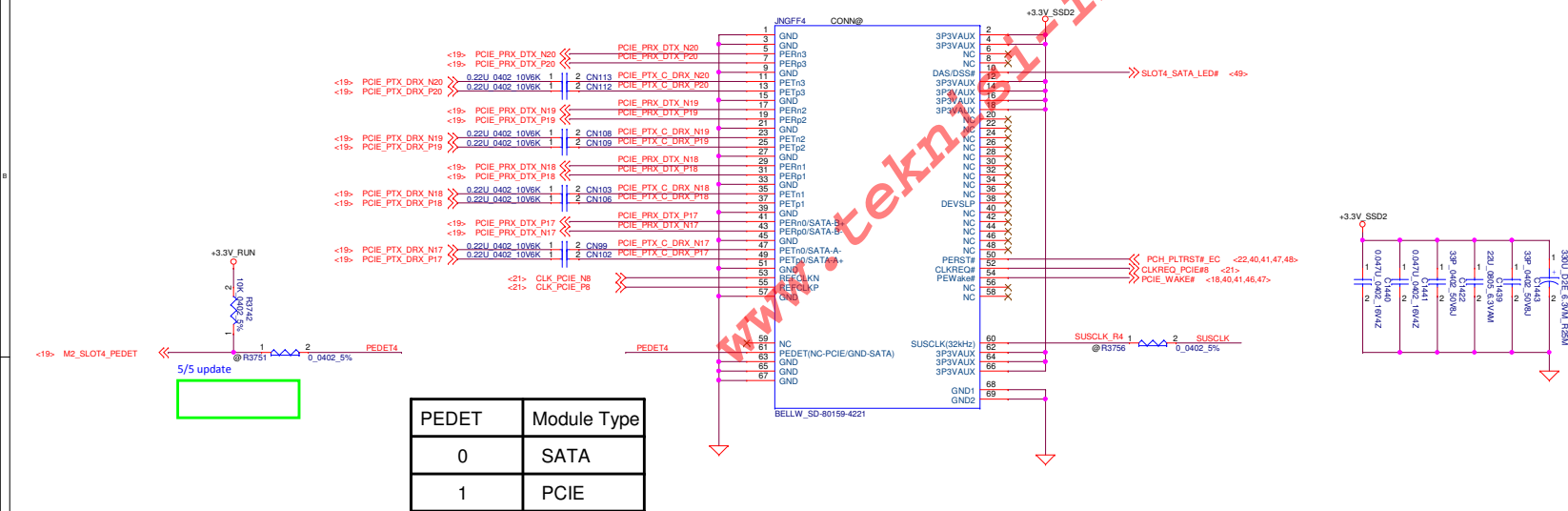
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SSD NGFF slot_3 Key M



SSD NGFF slot_4 Key M



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M.2 Card-2/2

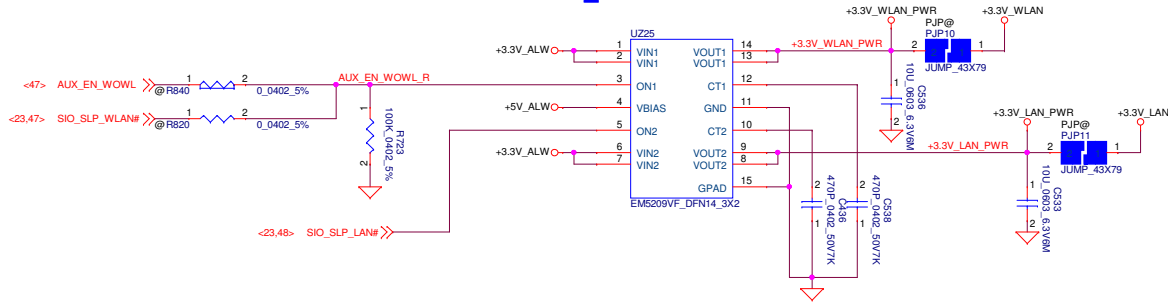
LA-E321P

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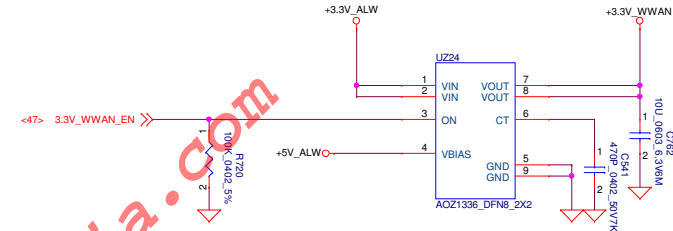
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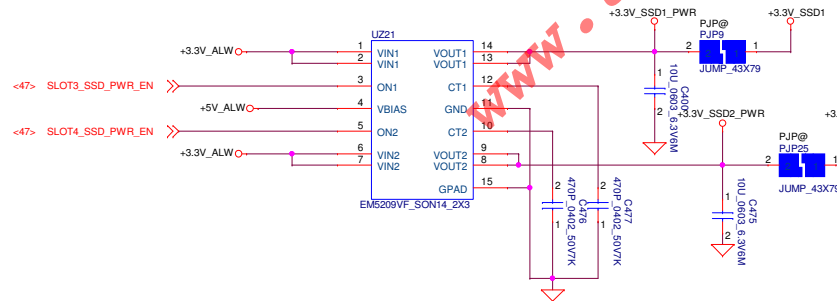
Power Control for M.2 slot 1. & +3.3V_RUN Source



Power Control for M.2 slot 2.



Power Control for M.2 slot 3. Source Power Control for M.2 slot 4. Source



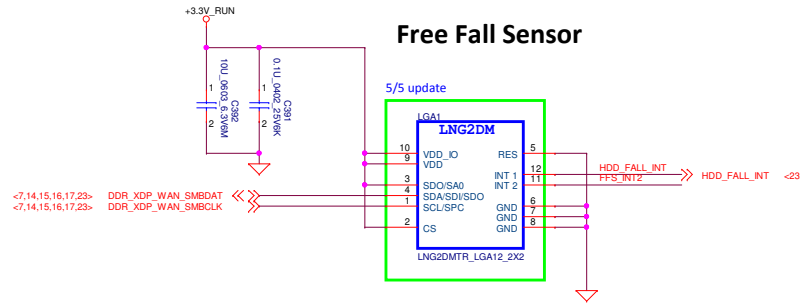
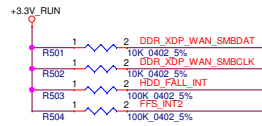
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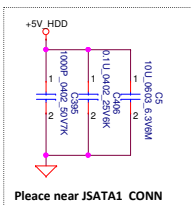
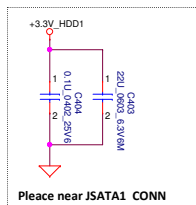
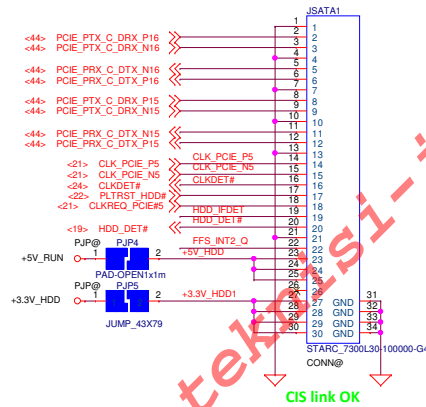
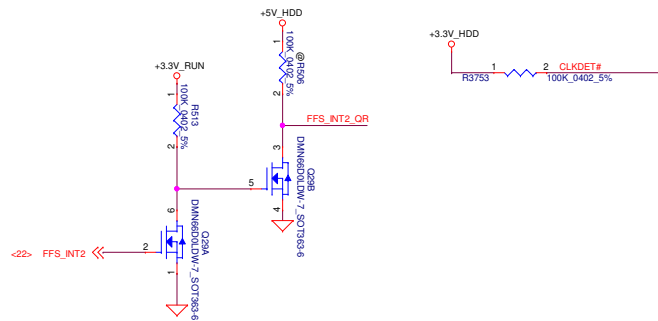
M.2 Card PWR

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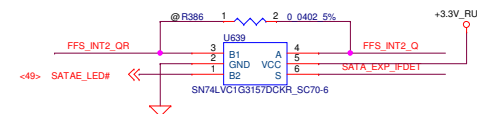
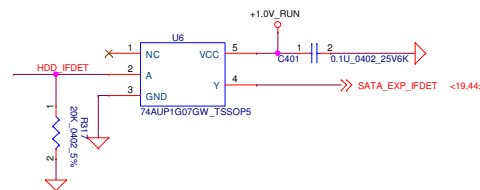
HDD1 CONN



HDD_IFDET	DEVICE interface
0	SATA
1	PCIE

SATA_EXP_IFDET	DEVICE interface
0	SATA
1	PCIE

SATA_EXP_IFDET	channel on
0	A-->B1
1	A-->B2

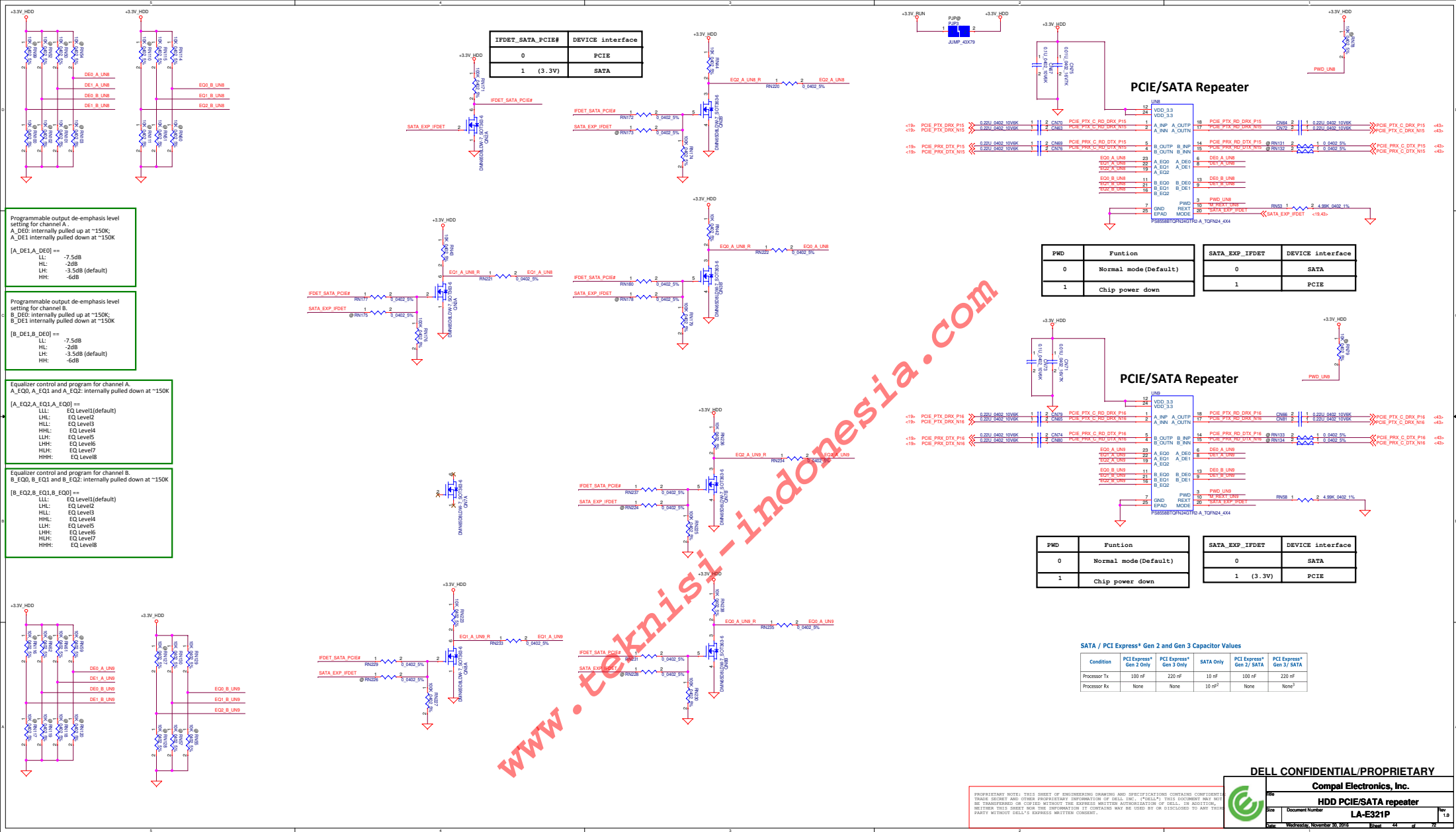


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USB/Codec/Card reader IO/B

Display daughter /B

Right Side JUSB1-----

Right Side JUSB2

Right Side JUSB3

TO TBT

TO DP

Footprint change to "-S"

Footprint change to "-S"

Power Button CONN

Power Switch for debug

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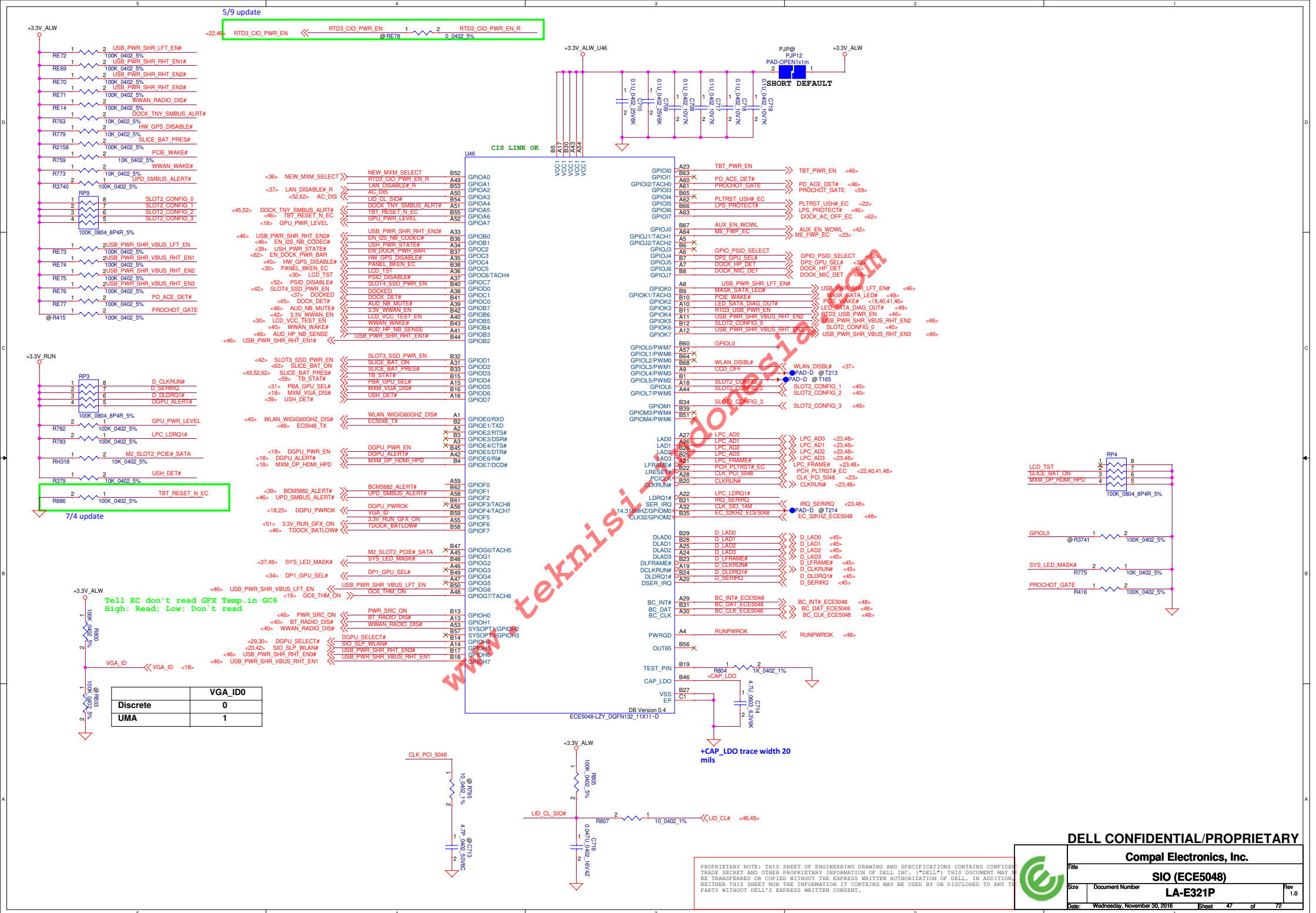
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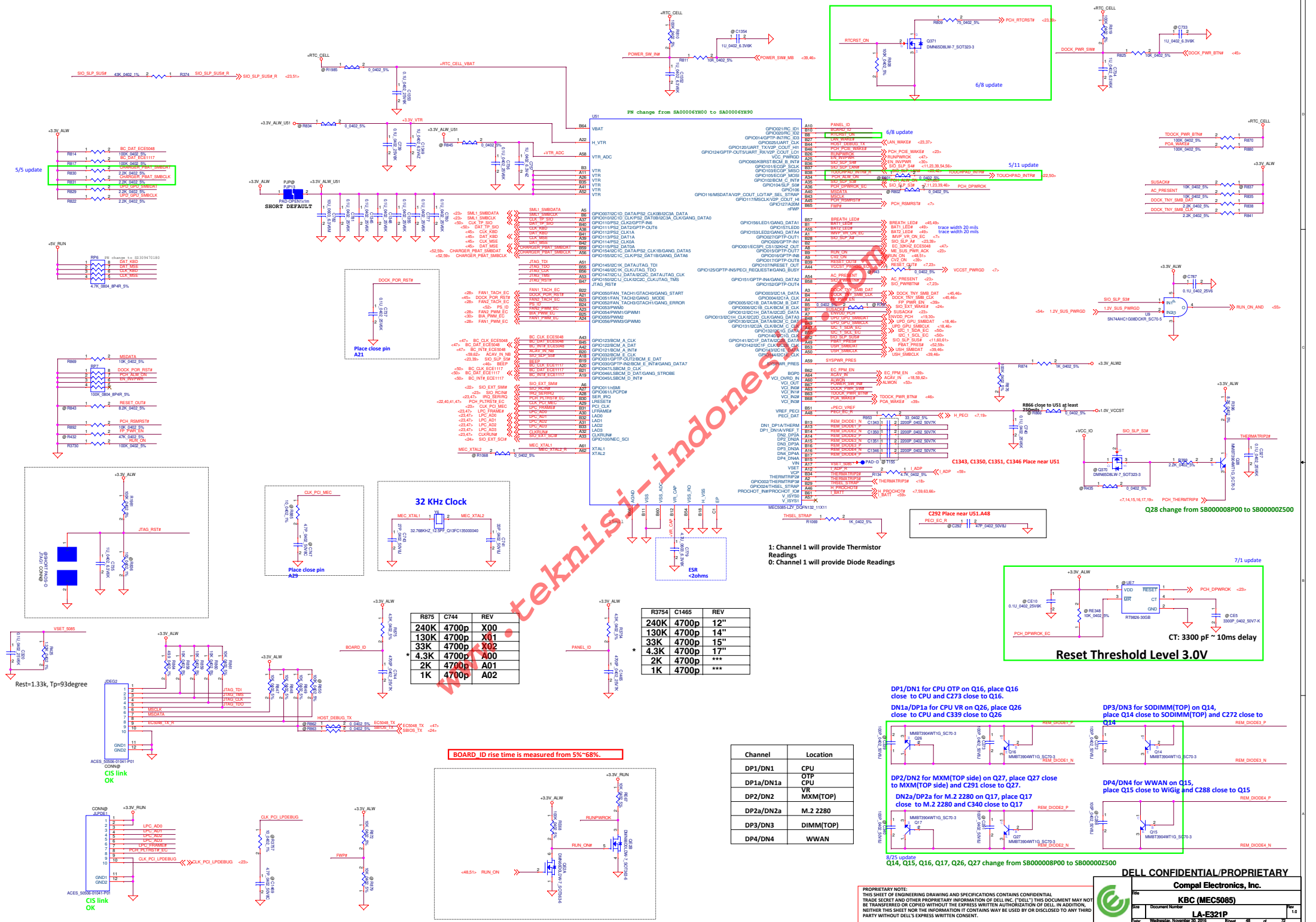
IO / PWR Button

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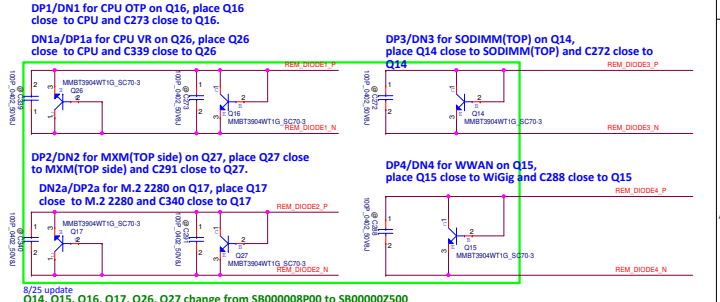




R875	C744	REV
240K	4700p	X00
130K	4700p	X01
33K	4700p	X02
4.3K	4700p	A00
2K	4700p	A01
1K	4700p	A02

R3754	C1465	REV
240K	4700p	12"
130K	4700p	14"
33K	4700p	15"
4.3K	4700p	17"
2K	4700p	***
1K	4700p	***

Channel	Location
DP1/DN1	CPU
DP1a/DN1a	OTP
DP2/DN2	CPU
DP2a/DN2a	VR
DP2a/DN2a	VR
DP2a/DN2a	VR
DP3/DN3	VR
DP3/DN3	VR
DP3/DN3	VR
DP4/DN4	VR
DP4/DN4	VR
DP4/DN4	VR



HDD LED

Breath LED

BREATH_LED TOP view.

BREATH_LED side view.

LED Circuit Control Table		
	SYS_LED_MASK#	LID_CL#
Mask All LEDs (Sniffer Function)	0	X
Mask Base MB LEDs (Lid Closed)	1	0
Do not Mask LEDs (Lid Opened)	1	1

BATT LED

To LED/B Conn

Fiducial Mark

FD1

FIDUCIAL MARK-D

FD2

FIDUCIAL MARK-D

FD3

FIDUCIAL MARK-D

FD4

FIDUCIAL MARK-D

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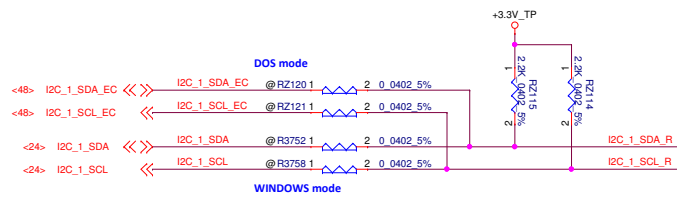
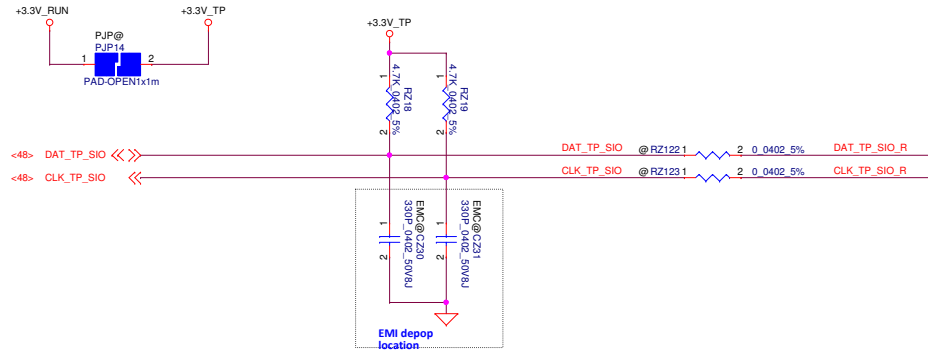
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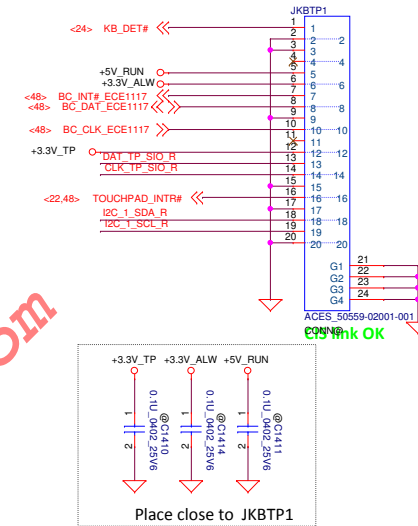
LED / Screw hole

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Touch Pad



Keyboard



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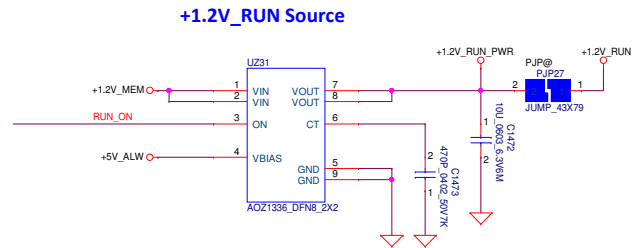
KB / TP / RSMRST#

LA-E321P

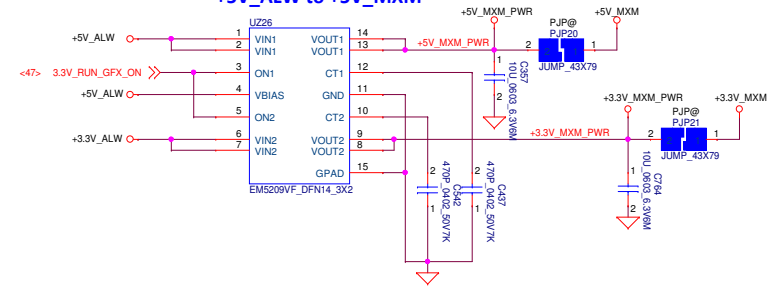
Thursday, December 08, 2016

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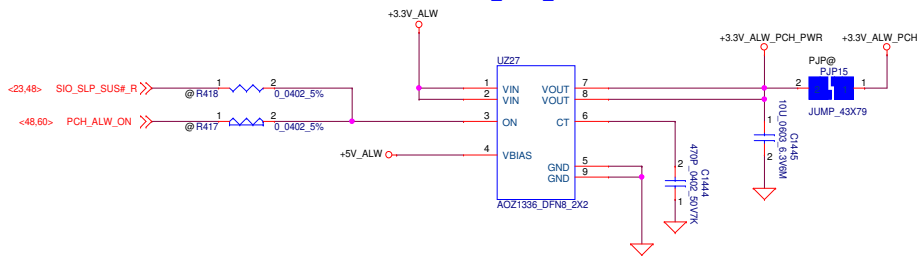
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**+3.3V_ALW to +3.3V_MXM
+5V_ALW to +5V_MXM**

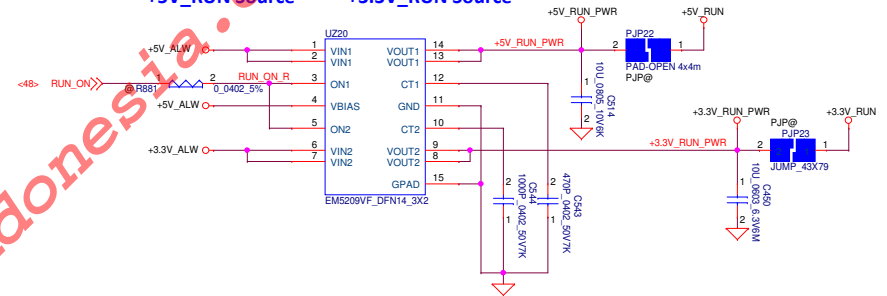


+3.3V_ALW_PCH Source

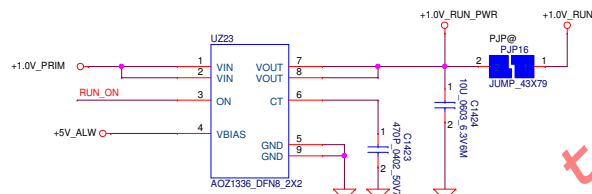


+5V_RUN Source

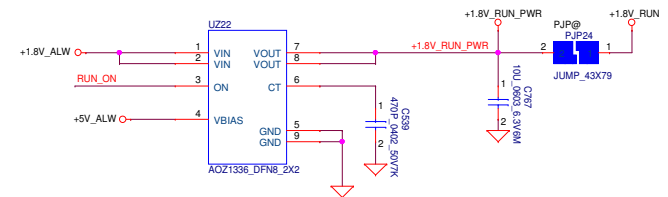
+3.3V_RUN Source



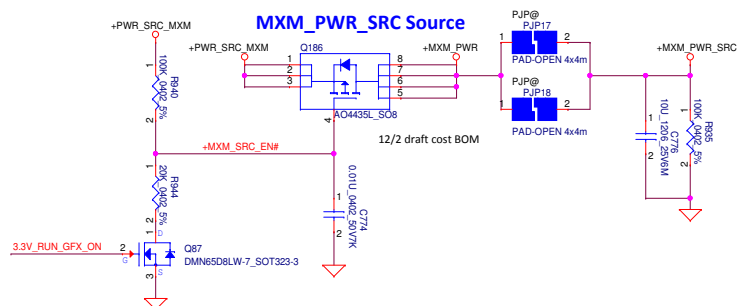
+1.0V_PRIM to +1.0V_RUN



+1.8V_RUN Source



MXM_PWR_SRC Source



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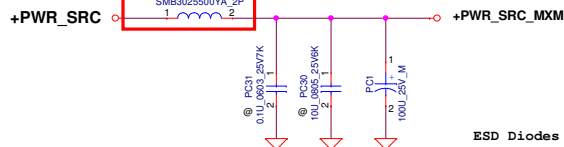
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Power Control

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EMI Part (47.1)



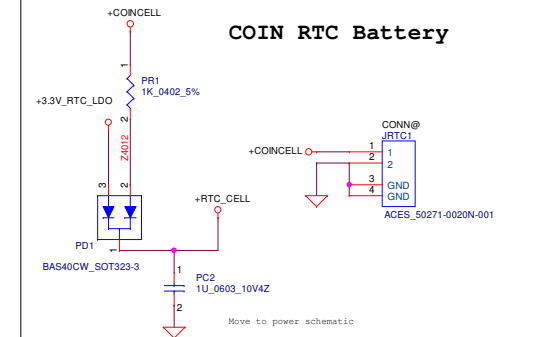
EVT change item from Miramar schematic

DVT1.0 change item

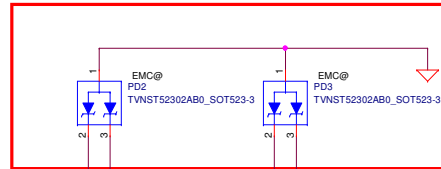
DVT2.0 change item

Pilot build change item

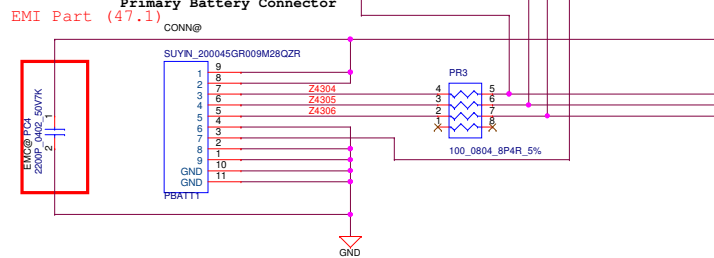
COIN RTC Battery



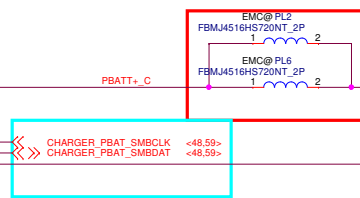
ESD (47.2)



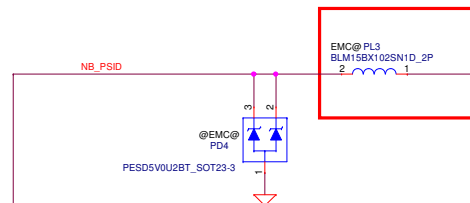
Primary Battery Connector



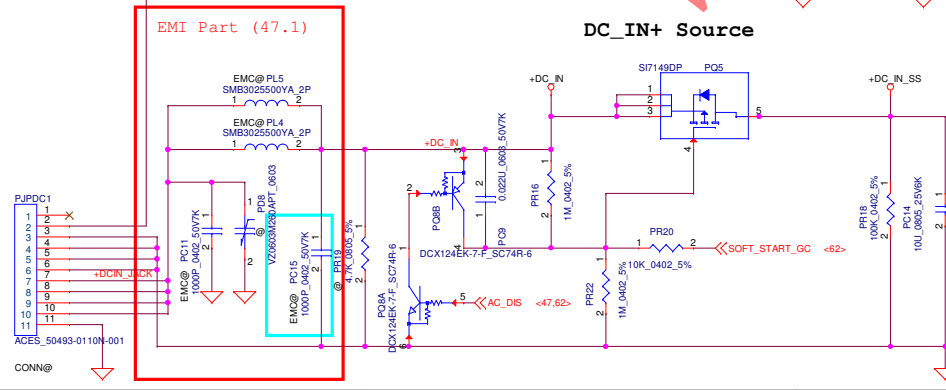
EMI Part (47.1)



EMI Part (47.1)



DC_IN+ Source



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Compal Electronics, Inc.

+DCIN

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+PWR_SRC

EMI Part (35.33)

+1.2V_MEN_P

EMI Part (35.33)

1.235Volt +/- 5%
TDC: 9.13 A
Peak Current: 13.04 A
OCP current: 15.65A
Rds (on): 3.5m ohm(max)
Choke DCR 3.5mohm(max)

11/16 PQ201,PQ202 BOM control with X76 for different vendor

NK0DDR@
PQ201
PK616BA PDFN8-5

NK0DDR@
PQ202
PK632BA PDFN8-5

Mode	S3	S5	+1.35V_MEN	+V_DDR_REF	+0.675V_P
S5	L	L	off	off	off
S3	L	H	on	on	off (Hi-Z)
S0	H	H	on	on	on

0.675Volt +/- 5%
TDC 1.05A
Peak Current 1.5A
OCP Current 1.8A

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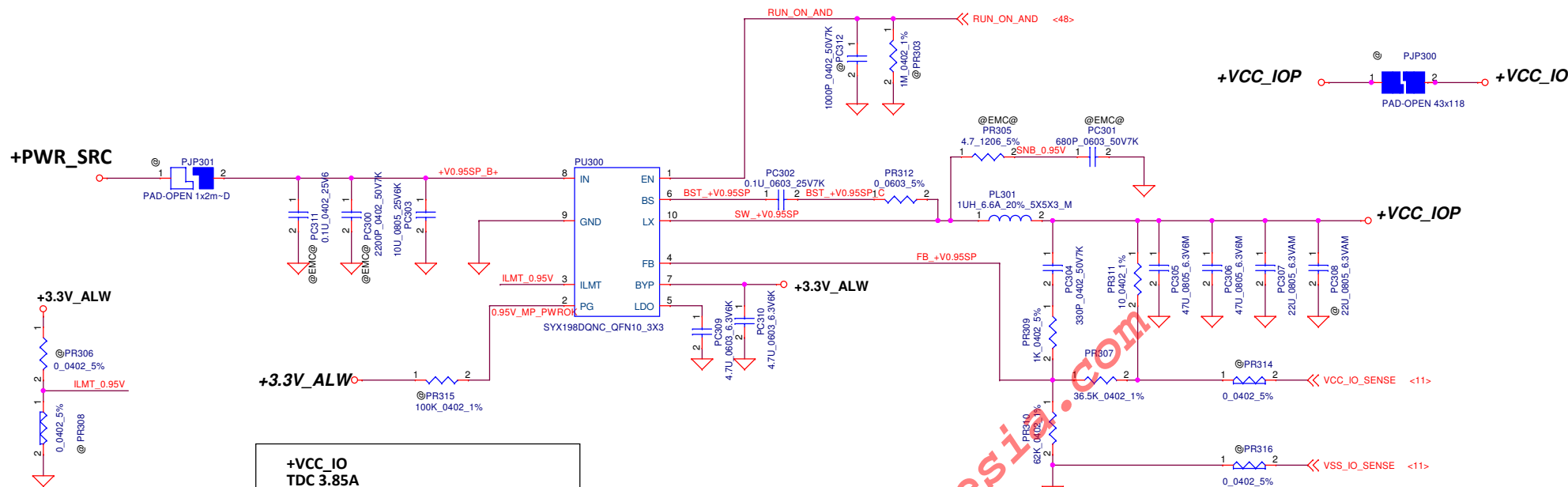


Compal Electronics, Inc.

1.2VP/0.6VSP

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+VCC_IO
TDC 3.85A
Peak Current 5.5 A
OCF Current 8 A
TYP MAX
Choke DCR 13.0mohm , 14.0mohm

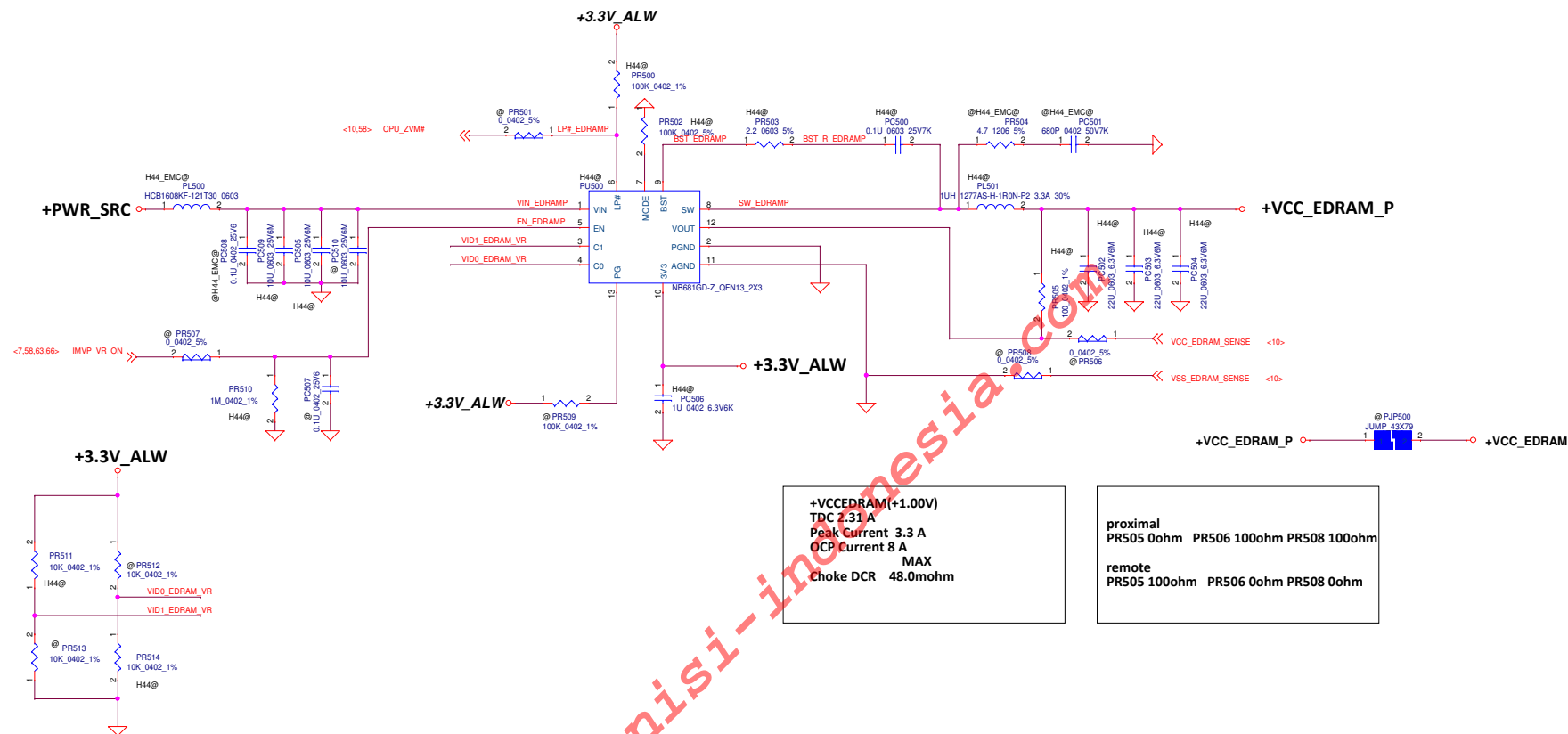
proximal
PR311 0 ohm PR314 10 ohm PR316 10 ohm
remote
PR311 10 ohm PR314 0 ohm PR316 0 ohm

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Compal Electronics, Inc.		
Title		
+VCC_IO 0.95V		
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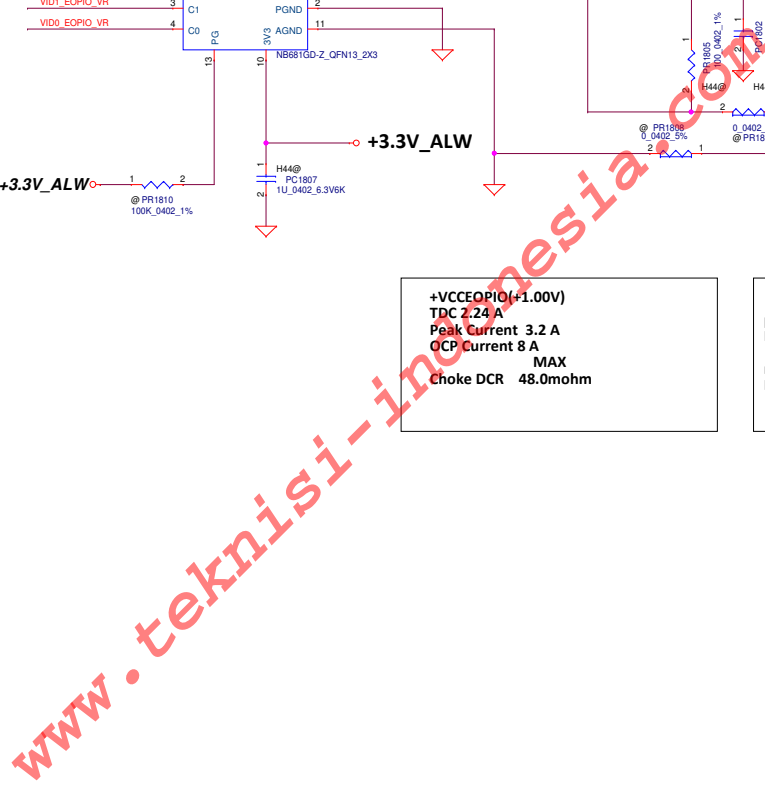
+VCCEDRAM, 1V

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Rev 0.3

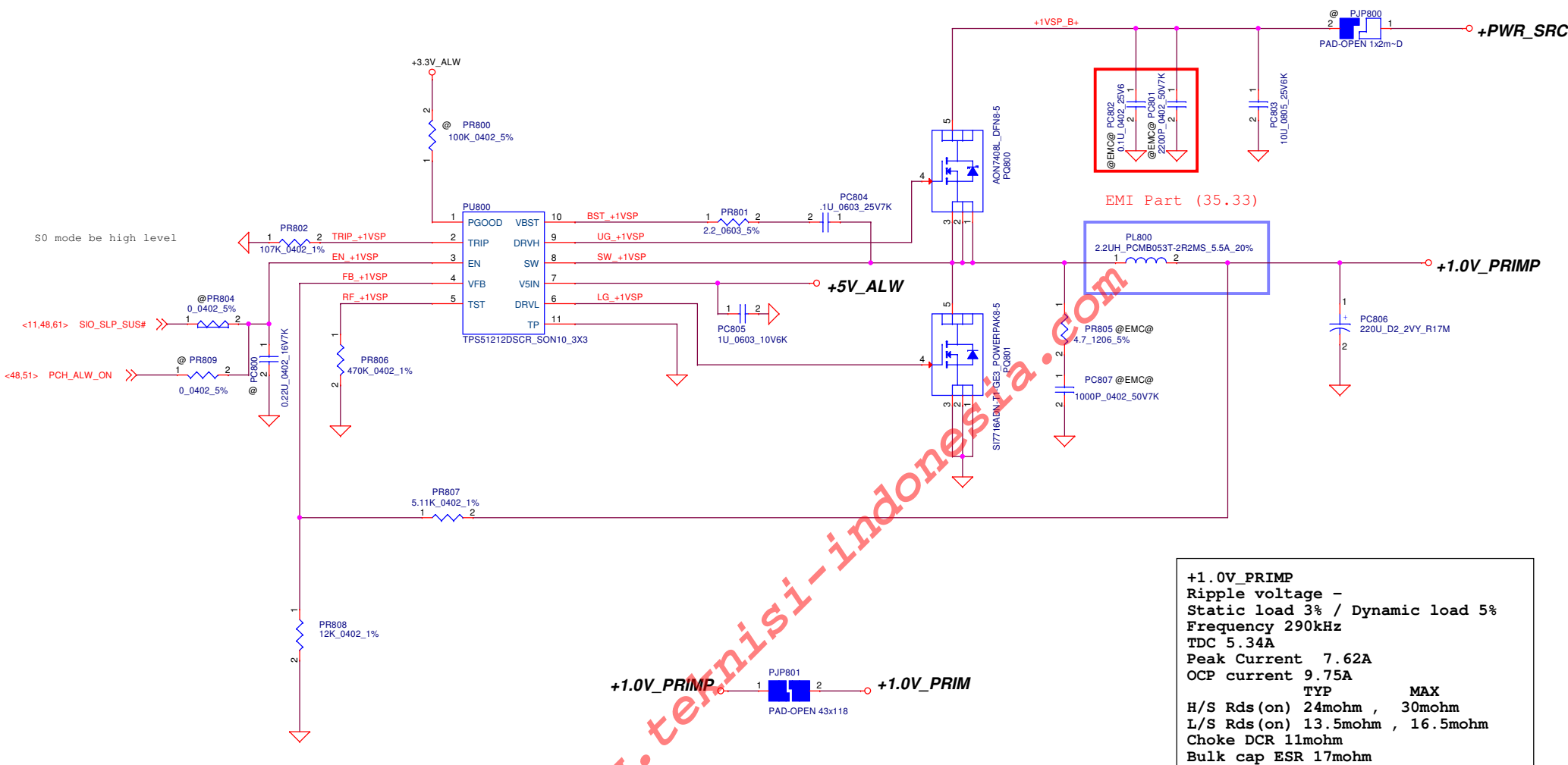
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+VCEOPIO(+1.00V)
 TDC 2.24 A
 Peak Current 3.2 A
 OCP Current 8 A
 MAX
 Choke DCR 48.0mohm

```
proximal
PR1805 0ohm  PR1806 100ohm PR1808 100ohm
remote
PR1805 100ohm PR1806 0ohm PR1808 0ohm
```

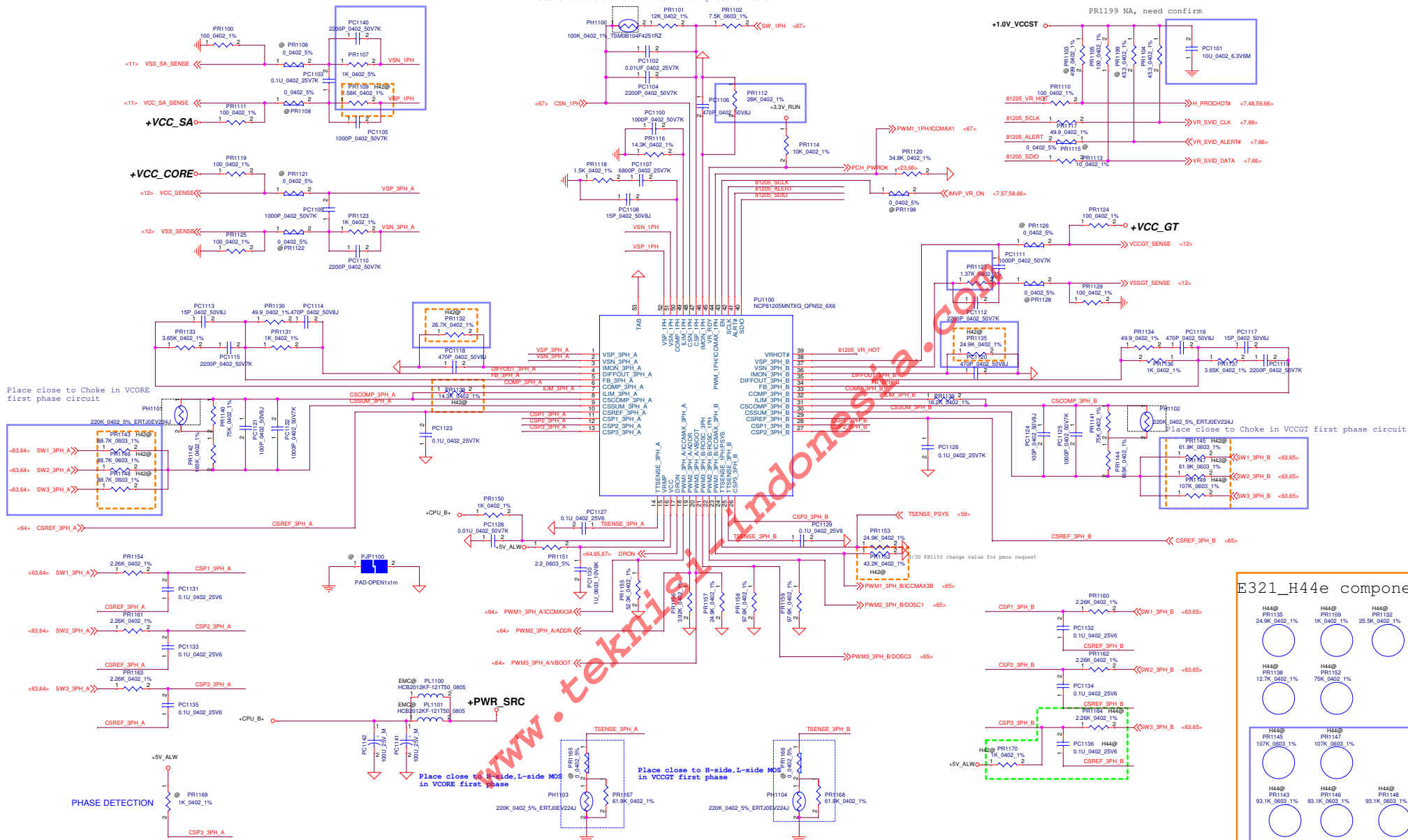
+1.0V PRIM		
Ripple voltage -		
Static load 3% / Dynamic load 5%		
Frequency 290kHz		
TDC 5.34A		
Peak Current 7.62A		
OCP current 9.75A		
	TYP	MAX
H/S Rds(on)	24mohm	30mohm
L/S Rds(on)	13.5mohm	16.5mohm
Choke DCR	11mohm	
Bulk cap ESR	17mohm	

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Title		
+1.0V PRIM		
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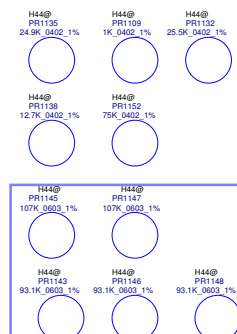
Place close to Choke in VCCSA first phase circuit



Place close to Choke in VCCORE first phase circuit


Place close to Choke in VCCGT first phase circuit

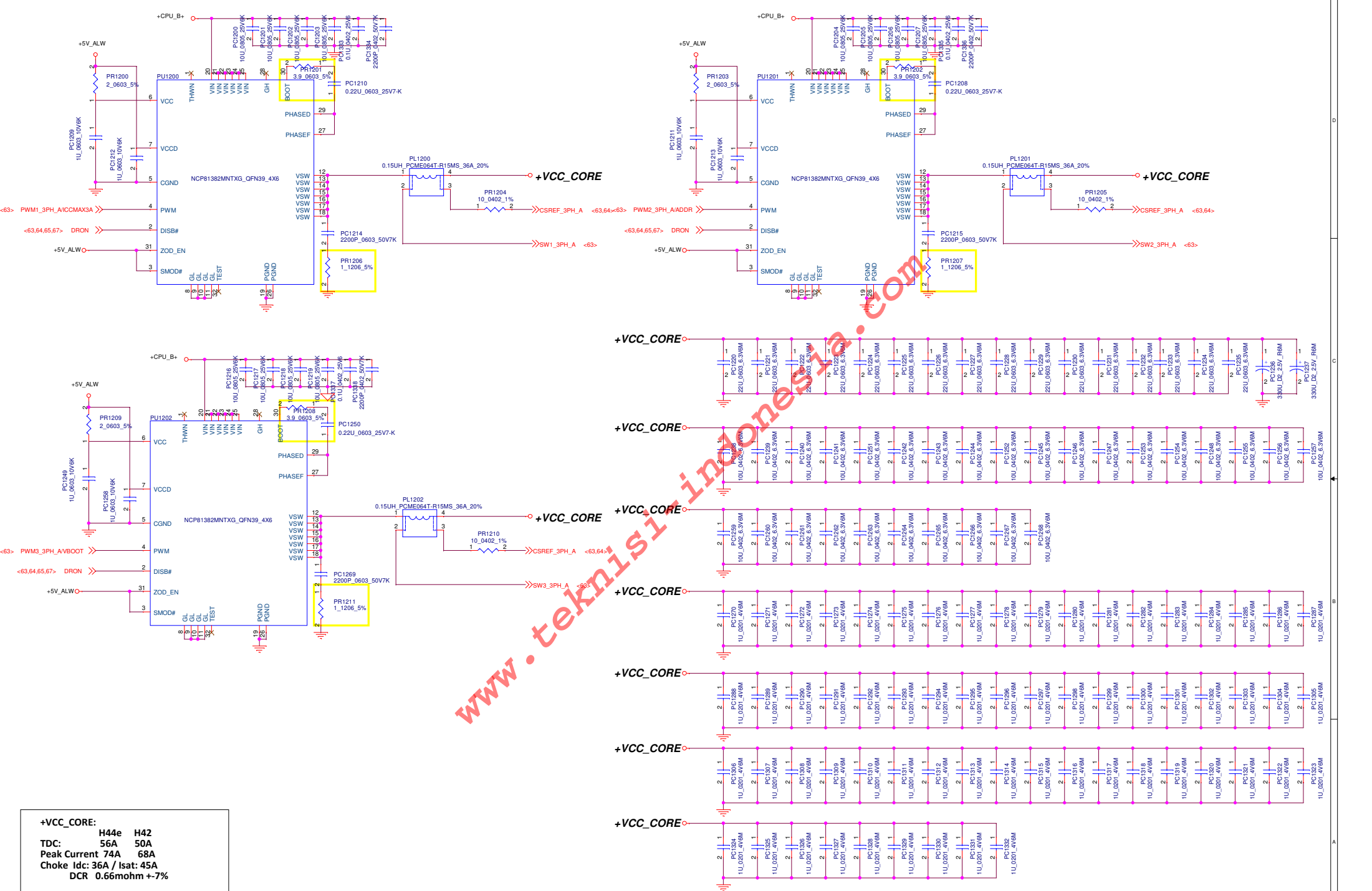
E321_H44e component



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Title		+VCCORE	
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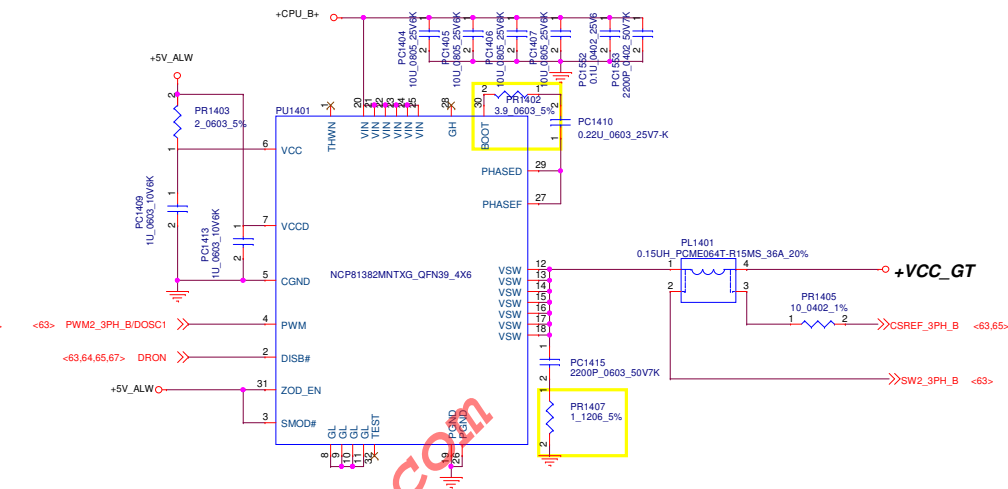


+VCC_CORE:
H44e H42
TDC: 56A 50A
Peak Current 74A 68A
Choke Idc: 36A / Isat: 45A
DCR 0.66mohm +7%

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		+VCC_CORE	
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[illegible]

+VCC_GT:	H44e	H42
TDC:	70A	25A
Peak Current	94A	55A
Choke Idc:	36A	Isat: 45A
DCR	0.66mohm +-7%	

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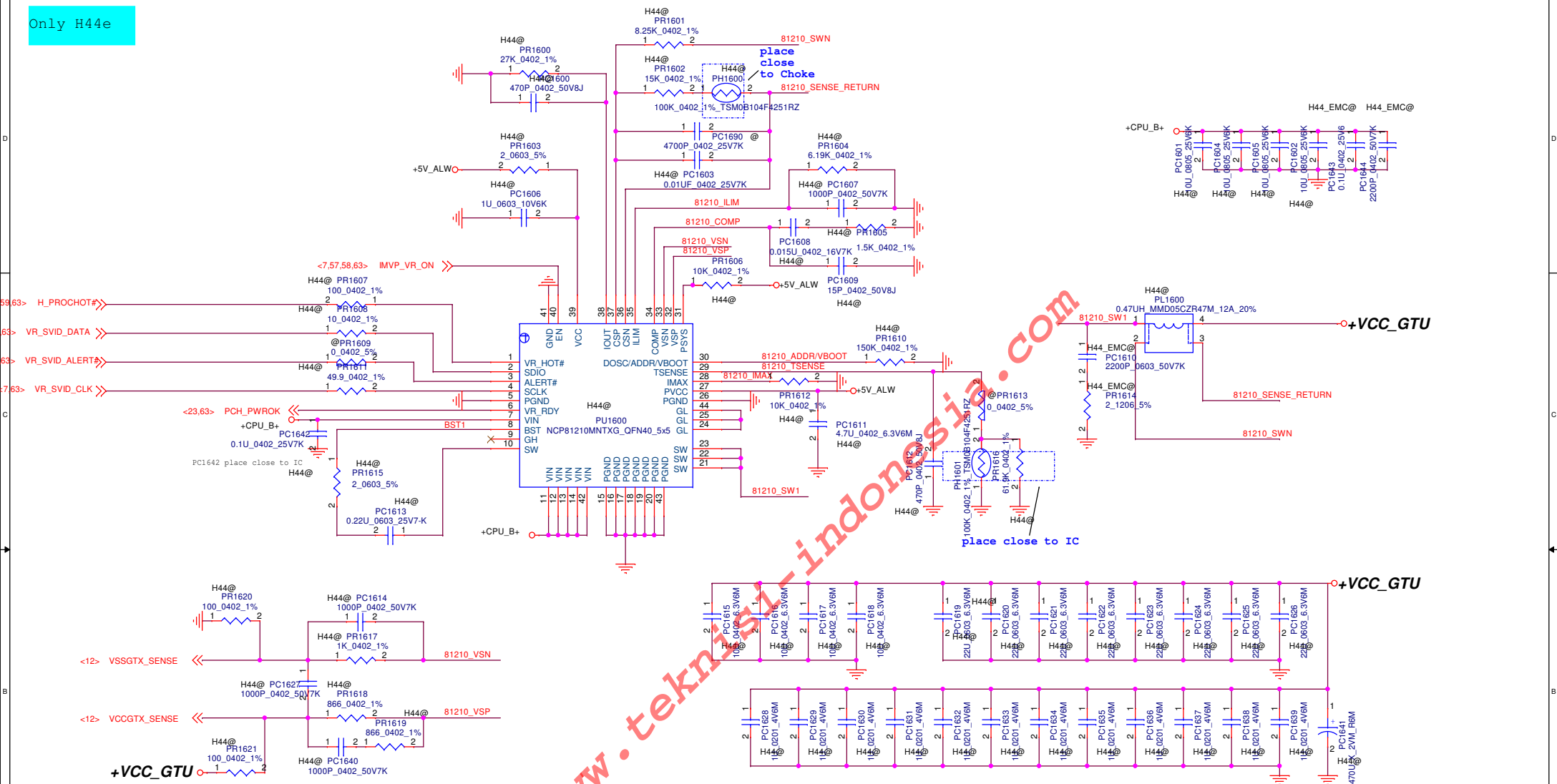
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+VCC GT

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Title			
+VCC GT			
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Only H44e



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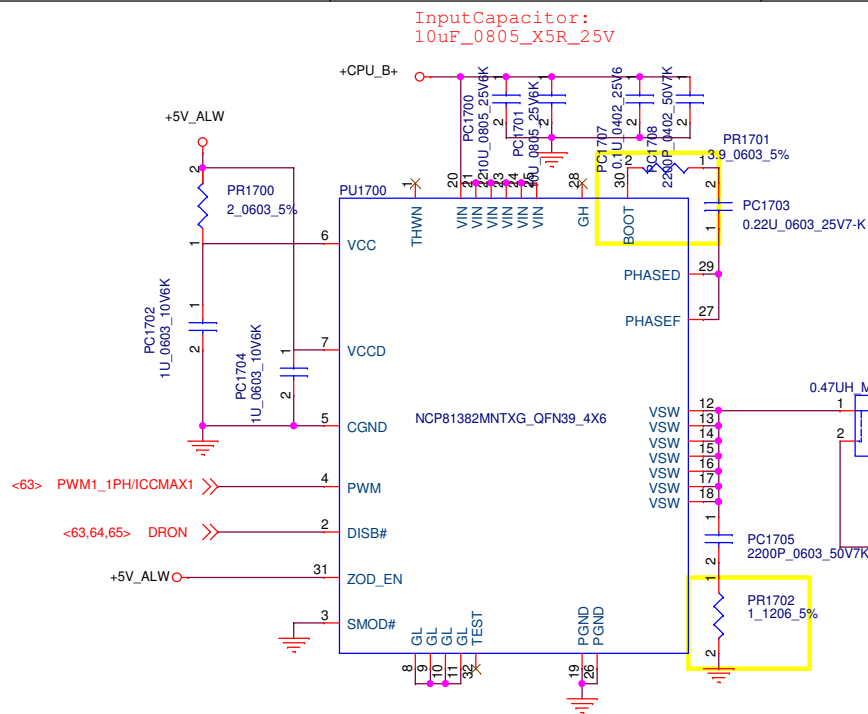
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+VCC_GTX

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Total VCORE Output
Capacitor:
8 X 22uF_0603_X5R

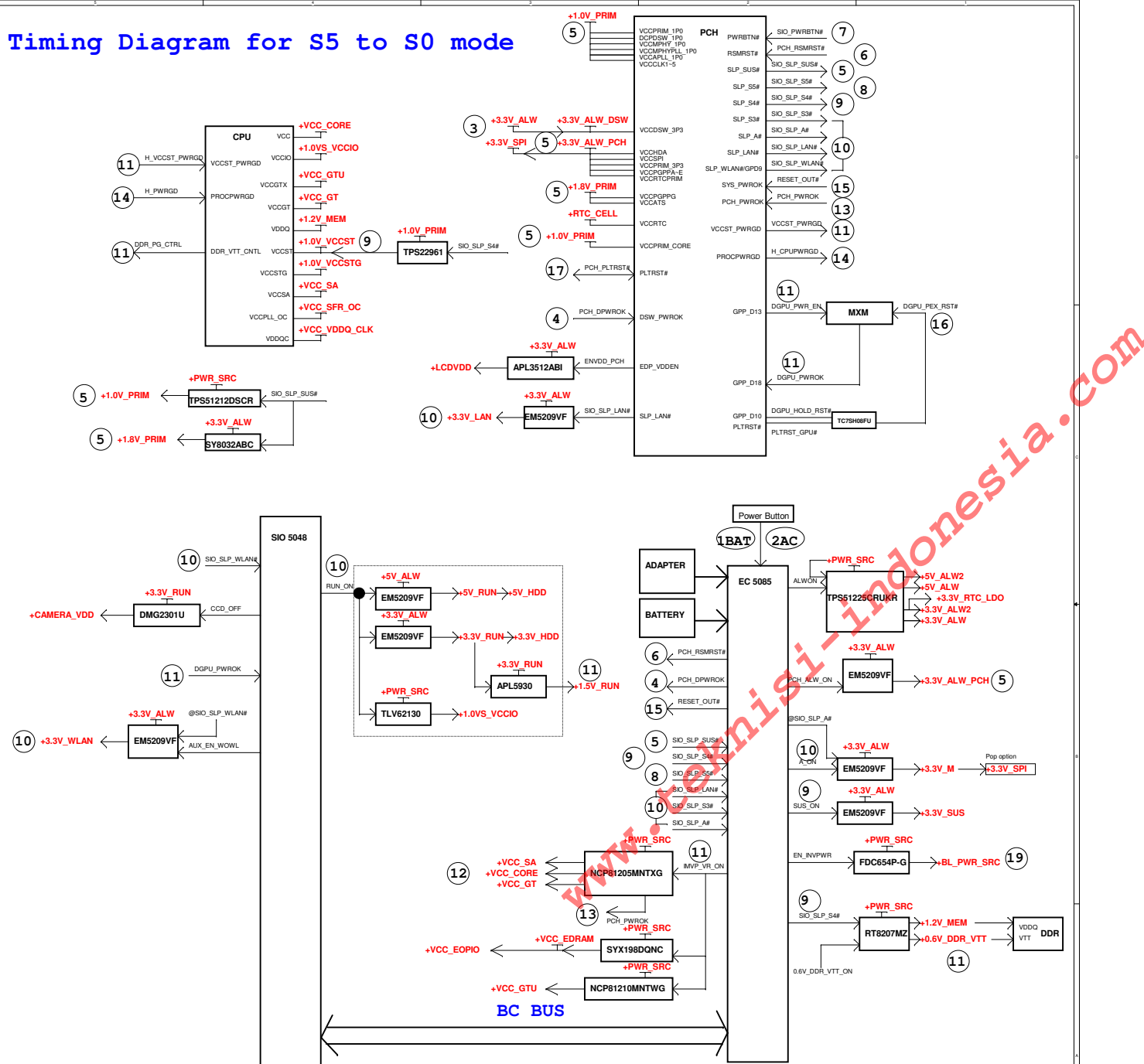
+VCC_SA
TDC 7.77A
Peak Current 11.1 A
OCP Current 13.32 A
Choke Idc: 12.2A / Isat: 16A
DCR 6.2mohm +-5%

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		Compal Electronics, Inc.	
		Title +VCC_SA	
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Timing Diagram for S5 to S0 mode



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Version Change List (P. I. R. List)

Item	Page#	Title	Date	Request Owner	Issue Description	Solution Description	Rev.
1	39	HW	2016/06/07	Compal	System cannot detect USH/B	Change RZ72 to 0ohm_short for load SW power to turn on +3.3V_CV2, +3.3V_FPM	0.2 (X01)
2	33	HW	2016/06/07	Compal	Mini DP can not display	Change HD3SS214 operate mode change from standby mode to normal mode, pop R107, depop R108	0.2 (X01)
3	39	HW	2016/06/07	Compal	Reverse for version B TPM IC design	Reverse RZ124, contact from SIO_SLP_S0# to TPM_LPM#	0.2 (X01)
4	14, 17	HW	2016/06/07	Compal	Change 330uf cap placement	Pop CD14, de-pop CD61	0.2 (X01)
6	48	HW	2016/06/08	Compal	For press power button over 20 sec, EC can sent RTCRST_ON to reset RTC	add R808, R809, Q371, and connect R808.1, Q371.2 to U51.B8	0.2 (X01)
7	38	HW	2016/06/08	Compal	C481 package change	Change from 0603 to 0402	0.2 (X01)
8	19	HW	2016/06/28	Compal	TBT_CIO_PLUG_EVENT# pull up change from +3.3V_ALW to +3.3V_ALW_PCH for power leakage	TBT_CIO_PLUG_EVENT# add RH366 pull to +3.3V_ALW_PCH, de-pop RH341	0.2 (X01)
9	46	HW	2016/06/28	Compal	To prevent damage with Miramar I/O board	Rotate JIO1 180 degree	0.2 (X01)
10	48	HW	2016/07/01	Compal	Board ID resistor value change	R875 change from 240k to 130k	0.2 (X01)
11	48	HW	2016/07/01	Compal	reserve for DPWROK sequence	Align BR team, add UE7, CE10, RE348, CE5	0.2 (X01)
12	39	HW	2016/07/01	Compal	USH_PWR_STATE voltage level keep high	change RZ10 from 1M to 100Kohm, depop DZ3, pop RZ76	0.2 (X01)
13	40	HW	2016/07/04	Compal	leverage X8-reserved 0 ohm on COEX1~3 between WWAN and WLAN	Add reserve RZ125, RZ126, RZ127	0.2 (X01)
14	47	HW	2016/07/04	Compal	leverage X8-TBT_RESET_N_EC add R886 PD 100Kohm	Add R886	0.2 (X01)
15	39	HW	2016/07/04	Compal	TPM leverage X8	change RZ111 from 0ohm-short to 0ohm, depop RZ111, RZ112, RZ82, QZ2, pop RZ124	0.2 (X01)
16	25	RF	2016/07/05	Compal	5.76G noise mitigation	RH363 and RH362 change from 0ohm to BLM15GA750SN1	0.2 (X01)
17	33	HW	2016/07/05	Compal	U636 HD3SS214ZQER footprint incorrect	Swap U636 pin E1, E2	0.2 (X01)
18	7	HW	2016/08/08	Compal	Design Guide	RC316 change from 1.5k to 3k	0.3 (X02)
19	50	HW	2016/08/08	Compal	Touchpad riseing time fail	Change RZ114, RZ115 from 4.7k to 2.2k	0.3 (X02)
20	21	HW	2016/08/08	Compal	Crystal EA test	CH4, CH5 change from 18pf to 15pf	0.3 (X02)
21	18, 21	HW	2016/08/25	Compal	add CLK_REQ# isolation for N17P/N17E MXM card	change QH3 to Q6 and connect Q6.1 to CLKREQ_PEG#0, Q6.2 to DGPU_PWROK, Q6.3 to MXM_CLK_REQ#, depop R1978	0.3 (X02)
22	31	HW	2016/08/25	Compal	Dock port1 DP test	Depop R99	0.3 (X02)
23	46	HW	2016/08/25	Compal	support USB3.0 wake in S3	JIO1.37 change from +3.3V_RUN to +3.3V_ALW	0.3 (X02)
24	18, 47	HW	2016/08/25	Compal	support UMA sku	add @R1973 between UH1.T45 and U46.B59, depop R803, pop R800	0.3 (X02)
25	39	HW	2016/08/25	Compal	add USH protect circuit for EC	add DZ4, @DZ5, @DZ6, DZ7, @DZ8, RZ128, @RZ129, UZ32, @RZ130, RZ131-RZ134, CZ98-CZ102, remove @RZ70, @RZ73, @RZ74, @RZ75, @RZ76, @RZ77, @RZ78, @RZ79, @RZ80, @RZ81, @RZ82, @RZ83, @RZ84, @RZ85, @RZ86, @RZ87, @RZ88, @RZ89, @RZ90, @RZ91, @RZ92, @RZ93, @RZ94, @RZ95, @RZ96, @RZ97, @RZ98, @RZ99, @RZ100, @RZ101, @RZ102, @RZ103, @RZ104, @RZ105, @RZ106, @RZ107, @RZ108, @RZ109, @RZ110, @RZ111, @RZ112, @RZ113, @RZ114, @RZ115, @RZ116, @RZ117, @RZ118, @RZ119, @RZ120, @RZ121, @RZ122, @RZ123, @RZ124, @RZ125, @RZ126, @RZ127, @RZ128, @RZ129, @RZ130, @RZ131, @RZ132, @RZ133, @RZ134, @RZ135, @RZ136, @RZ137, @RZ138, @RZ139, @RZ140, @RZ141, @RZ142, @RZ143, @RZ144, @RZ145, @RZ146, @RZ147, @RZ148, @RZ149, @RZ150, @RZ151, @RZ152, @RZ153, @RZ154, @RZ155, @RZ156, @RZ157, @RZ158, @RZ159, @RZ160, @RZ161, @RZ162, @RZ163, @RZ164, @RZ165, @RZ166, @RZ167, @RZ168, @RZ169, @RZ170, @RZ171, @RZ172, @RZ173, @RZ174, @RZ175, @RZ176, @RZ177, @RZ178, @RZ179, @RZ180, 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Version Change List (P. I. R. List)

Item	Page#	Title	Date	Request Owner	Issue Description	Solution Description	Rev.
27	45	HW	2016/08/31	Compal	add Docking protect circuit for EC	Add D101,@R210	0.3 (X02)
28	48	HW	2016/08/31	Compal	Board ID resistor value change	R875 change from 130k to 33k	0.3 (X02)
29	38	HW	2016/09/05	compal	EMI EA	change C485 from 150pF to 10pF	0.3 (X02)
30	39	HW	2016/09/08	compal	leverage X8-change TPM MPN to NPCT650VB2YX	change U637 from SA00008EL70 to SA00008EL80	0.3 (X02)
31	39	HW	2016/09/08	compal	remove reserve component on USH	remove DZ3,change RZ76 to 0ohm_short	0.3 (X02)
32	11.12	HW	2016/09/08	compal	reduce ripple of +1.0V_VCCST,+1.0V_VCCSTG,+1.0V_PRIMP	change CZ82, CZ88, CC195,CC186,CZ63,CZ90 to 10uf_0402	0.3 (X02)
33	12,19	HW	2016/09/12	INTEL	PDG1.0	change RH73 from 43ohm to 13ohm,CC187,CC188,C189 from 22uF to 10uF	0.3 (X02)
34	33	HW	2016/10/14	compal	AMD MXM CARD,display icon SHOW 3 Display when plug lmonitor	Add R153,R154 PD on MXM_DPB_HPD,PCH_DPD_HPD	1.0 (A00)
35	48	HW	2016/10/14	compal	Board ID change to A00	change R875 from 33Kohm to 4.3Kohm	1.0 (A00)
36	48	HW	2016/10/14	compal	advance BTB connector connection	change J101 from QT50A01-29100-7H to QT50A01-29200-7H,J102 from QT50A61-29100-7H to QT50A61-29200-7H	1.0 (A00)
37	18	HW	2016/10/14	compal	reserve for NV request	Add R155 between U17.1 and U17.2,add R156 between U17.1 and ACAV_IN	1.0 (A00)
38	31	HW	2016/10/14	Compal	Dock port1 DP test	Pop R99	1.0 (A00)

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Compal Electronics, Inc.




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Version Change List (P. I. R. List)Page 1

Item	Page#	Title	Date	Request Owner	Issue Description	Solution Description	Rev.
1	52 57	POWER	4/29	COMPAL	change PBAT_SMBCLK,CHARGER_SMBCLK; PBAT_SMBDAT,CHARGER_SMBDAT net name for HW request	PBAT_SMBCLK,CHARGER_SMBCLK change to CHARGER_PBAT_SMBCLK; PBAT_SMBDAT,CHARGER_SMBDAT change to CHARGER_PBAT_SMBDAT	Rev.01
2	52	POWER	5/4	COMPAL	for EMC request , pop and change PC15 from 0.1U to 1000P	change PC15 from 0.1U(SE042104K80) to 1000P (SE074102K80)	Rev.01
3	52	POWER	5/4	COMPAL	for EMC request , pop and change PC15 from 0.1U to 1000P	change PC15 from 0.1U(SE042104K80) to 1000P (SE074102K80)	Rev.01
4	56	POWER	5/12	COMPAL	for DDR4 2400 current request, change output choke to support	EL400 change from SH000000YG00 (S COIL 1UH +-30% 2.8A 4X4X2 FERRITE) to SH000000IW00 (S COIL 1UH +-20% PCMB042T-1R0MS 4.5A)	Rev.01
5	54	POWER	7/1	COMPAL	for RAM issue , HW request to change from 1.2V to 1.235V	change PR204 from 12K(SD034120280) to 13K(SD034130280)	Rev.02
6	64 65 67	POWER	7/1	COMPAL	For FAE check,pop Dr.MOS EMC part and change bootstrap resistor to reduce the ringing of SW node	change PR1201 PR1202 PR1208 PR1401 PR1402 PR1701 from SD013200B80 (S RES 1/10W 2 +-5% 0603) to SD000000YH00 (S RES 1/10W 3.9 +-5% 0603)	Rev.02
7	64 65 67	POWER	7/11	COMPAL	For FAE check, change snubber resistor to reduce the ringing of SW node	change PR1206 PR1207 PR12011 PR1406 PR1407 PR1702 from SD001200B80 (S RES 1/4W 2 +-5% 1206) to SD011100B80 (S RES 1/4W 1 +-5% 1206)	Rev.02
8	59	POWER	7/22	COMPAL	For Temp voltage test , +DC_IN setting for ACAVIN_NB need less than 17.55V , so change PR737 to achieve	change PR737 from SD034665380(S RES 1/16W 665K +-1% 0402) to SD034634380(S RES 1/16W 634K +-1% 0402)	Rev.02
9	53	POWER	9/2	COMPAL	With compal rule , need to use even part to back to back for acoustic noise improvement so add 3.3V/5V input MLCC to achieve	change PC101,PC102 from SE000000QK00(S CER CAP 10U 25V K X5R 0805 H1.25) to SE0000006R80(S CER CAP 4.7U 25V K X5R 0805 H1.25) and add PC122,PC123 SE0000006R80(S CER CAP 4.7U 25V K X5R 0805 H1.25)	Rev.03


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Item	Page#	Title	Date	Request Owner	Issue Description	Solution Description	Rev.
10	63	POWER	9/2	COMPAL	Change SW to controller resisters size from 0402 to 0603 to improve initial voltage for FAE suggest	change PR1143,PR1146,PR1148 from 82.5K 0402(SD000002780) to 82.5K 0603(SD014825280) and PR1145,PR1147 from 56.2K 0402(SD000001580) to 56.2K 0603(SD014562280)	Rev.03
11	60 63	POWER	9/2	COMPAL	To improve HW side +1.0V_VCCST ,+1.0V_VCCSTG and +1.0V_VCCSFR output ripple , change 1.0V_PRIM choke and VCCST MLCC	Change PL800 from SH000002200 (S COIL 1UH +-20% 6.6A 5X5X3 MOLDING) to SH00000R810 (S COIL 2.2UH +-20% PCMB053T-2R2MS 5.5A) and PC1101 from SE00000G880 (S CER CAP 0.1U 25V K X5R 0402) to SE00000UD00 (S CER CAP 10U 6.3V M X5R 0402)	Rev.03
12	63	POWER	9/12	COMPAL	For SA Loadline and Iout improvement , modify parameter of VR ciruit from FAE suggestion	Pop PC1140 and change from 1000P (SE074102K80) to 2200P (SE074222K80); change PR1107 from short pad to 1K (SD028100180); change PR1109 from 1.43K (SD034143180) to 1.58K (SD00000S780); change PR1112 from 30K (SD034300280) to 28K (SD034280280)	Rev.03
13	63	POWER	9/14	COMPAL	For IA,GT Loadline and Iout improvement , modify parameter of VR ciruit from FAE suggestion	IA part Change PR1143,PR1146,PR1148 from 82.5K (SD014825280) to 88.7K (SD014887280); change PR1132 from 24.3K to 26.7K (SD034267280); GT part Change PR1145,PR1147 from 56.2K (SD014562280) to 61.9K (SD014619280); change PR1135 from 22.6K to 24.9K (SD034249280)	Rev.03
14	53 59 60	POWER	9/20	COMPAL	For Dell request , 3.3V/5V HS and LS MOS should be used with the same vender	High side MOS Change PQ100,PQ101,PQ800 from SB00000IA00 (S TR S1S412DN-T1-GE3 1N POWERPAK1212-8) to SB00000H800 (S TR AON7408L 1N DFN); Low side MOS Change PQ102,PQ103,PQ705 from SB00000N800 (S TR FDMC7692S 1N MLP) to SB000010U00 (S TR AON7752 1N DFN3X3EP)	Rev.03
15	53	POWER	9/26	COMPAL	For HW request , need to increase 5V output voltage from 5V to 5.08V to reduce PD output voltage drop	Change PR101 from SD034150280 (S RES 1/16W 15K +-1% 0402) to SD034154280 (S RES 1/16W 15.4K +-1% 0402)	Rev.03
16	63	POWER	9/26	COMPAL	To meet intel SPEC for GT voltage , need to modify parameter of VR circuit	Change PR1127 from SD034100180 (S RES 1/16W 1K +-1% 0402) to SD034137180 (S RES 1/16W 1.37K +-1% 0402)	Rev.03
17	53	POWER	11/11	COMPAL	For type C test , change FB resisters to rise output voltage from 5V to 5.156V	Change PR101 from SD034158280 (S RES 1/16W 15.8K +-1% 0402) to SD034154280 (S RES 1/16W 15.4K +-1% 0402) change PR104 from SD028102280 (S RES 1/16W 10.2K +-1% 0402) to SD034976180 (S RES 1/16W 9.76K +-1% 0402)	Rev.10
18	54	POWER	11/11	COMPAL	For 1.2V damage issue , upgrade high side MOS to improve	Change PQ201 from SB00000K300 (S TR SIRA72DP-T1-GE3 1N POWERPAK S08) to SB00000WY00 (S TR SIRA14DP-T1-GE3 1N POWERPAK S08)	Rev.10
19	54	POWER	11/16	COMPAL	For 1.2V damage issue , change HS/LS MOS from Vishay to Magnachop and 1.235V change back to 1.2V	Change PQ201 from SB00000WY00 (S TR SIRA14DP-T1-GE3 1N POWERPAK S08) to SB00001GP00 (S TR AON6380 1N DFN5X6-8); change PQ202 from SB00000WX00 (S TR SIRA06DP-T1-GE3 1N POWERPAKS0-8) to SB00001GK00 (S TR AON6314 1N DFN5X6-8) change PR204 from SD034130280 (S RES 1/16W 13K +-1% 0402) to SD034120280S RES 1/16W 12K +-1% 0402)	Rev.10

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